

MEDIATEK

everyday genius

MT7531 Reference Manual

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Document Revision History

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1.1	2019-07-10	Update BMU description Update interrupt description
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1 Memory Map

1.1 Top memory map

The top level memory map is shown as table below. For more memory information, please refer the section “Buffer Management Unit”.

Start Address	End Address	Size	Registers
0x0000	0x0fff	4096	ARL registers
0x1000	0x10ff	256	Scheduler registers
0x1100	0x1fff	3840	BMU registers
0x2000	0x20ff	256	Per-port ARL registers
0x3000	0x30ff	256	MAC registers
0x4000	0x47ff	2048	MIB registers
0x5000	0x51ff	512	Port 5 SGMII registers
0x6000	0x61ff	512	Port 6 SGMII registers
0x7000	0x77ff	2048	Switch system control registers
0x7800	0x79ff	512	Top registers
0x7c00	0x7eff	768	I/O registers

1.2 GPHY memory map

The GPHY related registers are listed in section “GPHY”.

2 Address Resolution Logic (ARL)

2.1 Introduction

Address Resolution Logic (ARL) supports 2K address table shared by MAC address, destination IP address and source IP address. When frame forwarding is performed on the address table, the MAC DA will be used to look up the MAC entry to get the destination port map, priority, VLAN ID, etc. At the same time, the MAC SA should be learned into the address table. When the incoming frame carries the IP multicast frame, the destination IP address will be used to look up the DIP entry. For IGMPv3 or MLDv2, SIP is also used to check the Source IP List. ARL also supports up to 4K IEEE 802.1Q port-based VLAN and 8 priority queues for advanced network management and QoS solutions. Using the VLAN feature, users can manage the broadcasted traffic efficiently. Through the priority queue mechanisms, ARL switches different kinds of traffic (e.g., normal data, expedited data, voice and video) according to the traffic characteristics and user's requirements and provides end users with a multimedia environment.

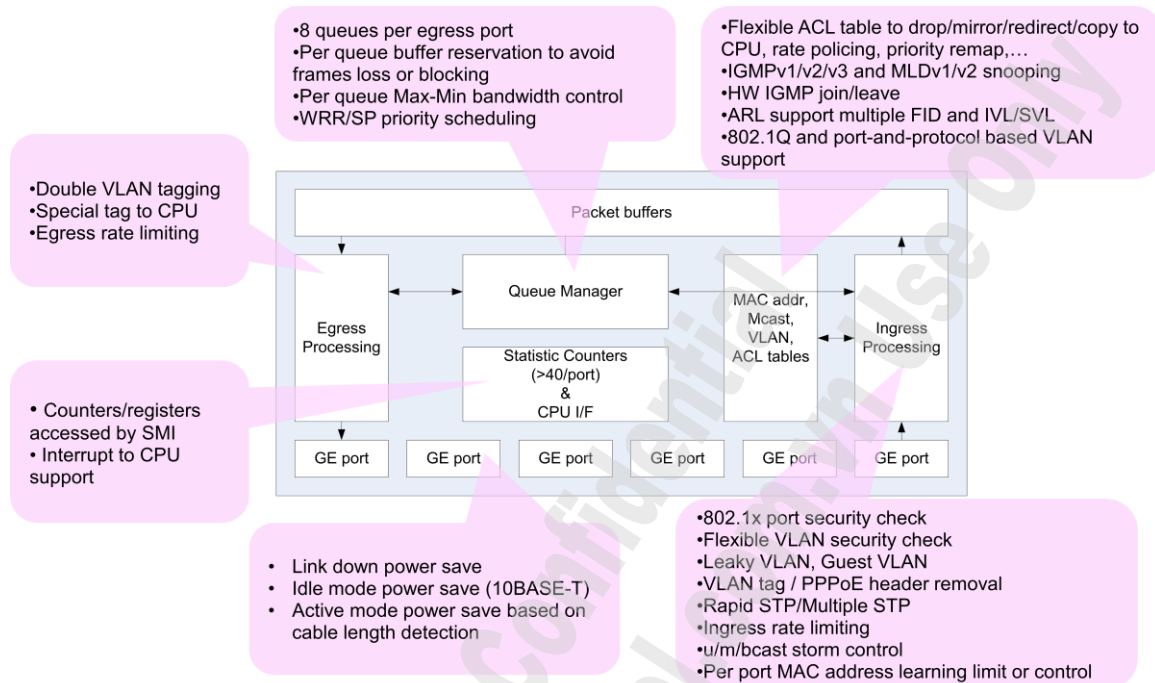
Although Ethernet switch or bridge is well-defined by IEEE Std.802.3, additional requirements are still needed for it to fit in future standards or to improve security, QoS, or policy control. ARL provides Access Control Logic (ACL) with the wire-speed control on the incoming frames. ACL Table includes 256 entries rule table and 128 entries rule control table.

2.2 Features

- Built-in address table with 2K MAC addresses which can support up to 8 filtering databases
 - Accessible by managing interface to keep static addresses
 - Support IVL/SVL based on FID from VLAN table
 - Programmable aging timer: no aging out, 10 ~ 1,000,000 seconds; default is 300 seconds
 - Configurable Address look-up algorithm. Address look-up based on the proprietary hashing algorithm, CRC16 or CRC32.
 - Support Collision Pool with 64 entries
- Up to 4K full VLAN entries with flexible support for IEEE 802.1Q and port-based VLAN
 - Support port-based, Tag-based, and up to 4 port-and-protocol based VLAN
 - Support per-port VLAN tag addition, removal, or leave unchanged
 - Provide special tag for CPU port
 - Support Per Egress port stack VLAN (Q in Q)
 - Support Per Egress port 1:1 and N:1 VLAN Translation
- Leaky VLAN based on port attribute, MAC address and ACL
- ACL Table includes 256 entries rule table and 128 entries rule control table
 - ACL Rule support layer 1 to layer 4. Rules include Port No., DA/SA, Ether Type, VLAN ID, IP Protocol, SIP/DIP, TCP/UDP, SP/DP and user-defined content

- Actions support mirror, redirect, dropping, priority adjustment, and traffic rate policing
- Optional per-port Enable/Disable of ACL function
- Optional setting of per-port action when ACL is mismatched
- IGMP/MLD snooping
 - Support IPv4 IGMP v1/v2/v3 snooping and IPv6 MLD v1/v2 snooping
 - Trap all IGMP and MLD packets to the CPU port. CPU writes the correct multicast entry to the lookup table via management interface
 - Support hardware IGMP(v1/v2) join and fast leave
 - Support partial hardware IGMPv3 and MLDv2 - IS_EX(), TO_EX(), TO_IN(). User-defined SIP Table for IGMPv3/MLDv2, SIP Table hardware auto learning is not supported.
- Support Spanning Tree port behavior configuration
 - IEEE 802.1w Rapid Spanning Tree
 - IEEE 802.1s Multiple Spanning Tree with up to 8 Spanning Tree instances
- Broadcast/Multicast/Unknown DA storm control/alert depending on the number of the frames received during a period of time to protect the system from being attacked by hackers
- Per port MAC Address learning control to protect the system from being attacked by hackers
 - Disable learning or aging for Per-port
 - Limit SA Learning number for Per-port
- Support IEEE 802.1x access control protocol and advanced security features
 - Access policy based on Port-based, MAC-based and guest VLAN
 - Access control based on ACL rules
 - Drop unknown Source MAC or Destination MAC address for Per-port
- PPPoE/PPP identifier and header removal for IP multicast packets
- Support Link Aggregation (Port Trunking)
 - Support maximum 3 aggregation group. Each aggregation group has 2 ports.
 - Configurable port setting for each aggregation group.
 - Configurable distribution scenario. Information used to assign conversations to aggregation ports is configurable. Including Source Port, MAC DA, MAC SA, Source IP Address, Destination IP Address, TCP/UDP Source Port and TCP/UDP Destination Port.

2.3 Block Diagram



ARL Function Blocks

2.4 Frame Classifications

2.4.1 Broadcast Frames

Broadcast Frames

FTAG	DA	Type	IPv4/IPv6 Protocol	Description
BC	FF-FF-FF-FF-FF-FF	-	-	Broadcast Frames
ARP	FF-FF-FF-FF-FF-FF	08-06	-	ARP Request Frames
	-	08-06	-	ARP Reply Frames
RARP	FF-FF-FF-FF-FF-FF	80-35	-	RARP Request Frames
	-	80-35	-	RARP Reply Frames

2.4.2 Multicast Frames

Multicast Frames

FTAG	DA	Type	IPv4/IPv6 Protocol	Description
MC	The 1st bit of MSB is 1'b1	-	-	Multicast Frames
IGMP	-	08-00	0x02	IGMP Message
IP_MULT	01-00-5E-xx-xx-xx	-	-	IP Multicast (UDP)
MLD	-	86-DD	0x00 0x3A	Hop-by-Hop ICMPv6 (MLDv2)
IPV6_MULT	33-33-xx-xx-xx-xx	-	-	IPv6 Multicast (UDP)
BPDU	01-80-C2-00-00-00	-	-	Bridge Group Address (BPDU)
REV_01	01-80-C2-00-00-01	-	-	Clause 31 (MAC Control) of IEEE Std 802.3
CONTROL (PAUSE)	-	88-08	-	Discarded
	01-80-C2-00-00-01 Or Unicast DA	88-08	Followed by 00-01	MAC Control -Pause Frame (< 1518 bytes) (Discarded)
REV_02	01-80-C2-00-00-02	-	-	Clause 43 (Link Aggregation) and Clause 57 (OAM) of IEEE Std 802.3
PAE	01-80-C2-00-00-03 Or Other	88-8E	-	IEEE Std 802.1X PAE address
REV_03	01-80-C2-00-00-03	--	-	
REV_UN	01-80-C2-00-00-04 ~05	-	-	Reserved for future standardization— media access method specific
	01-80-C2-00-00-06 ~0D	-	-	Reserved for future standardization— VLAN-aware Bridge specific
REV_OE	01-80-C2-00-00-0E			IEEE Std 802.1AB Link Layer Discovery Protocol multicast address

REV_UN	01-80-C2-00-00-0F			Reserved for future standardization— VLAN-aware Bridge specific
REV_10	01-80-C2-00-00-10			All LANs Bridge Management Group Address
REV_20	01-80-C2-00-00-20			GMRP Address
REV_21	01-80-C2-00-00-21			GVRP Address
REV_UN	01-80-C2-00-00-22 ~ 01-80-C2-00-00-xx	-	-	Reserved for future standardization

2.4.3 Unicast Frames

Unicast Frames

FTAG	DA	Type	Description
UC	The 1st bit of MSB is 1'b0	-	Unicast Frames
ARP	FF-FF-FF-FF-FF-FF	08-06	ARP Request Frames
	-	08-06	ARP Reply Frames
RARP	FF-FF-FF-FF-FF-FF	80-35	RARP Request Frames
	-	80-35	RARP Reply Frames

2.5 Switch L2/L3 Address Table

The switch has a 2K address table built in for packet look-up forwarding. All the entries can be shared and mixed by L2 MAC address or L3 IP address according to "TYPE" definition. When the entry is regarded as a MAC address table, it is used to forward packets by L2 DA and learn packets by L2 SA. When the entry is regarded as a DIP address table, it is used to process IGMP/MLD snooping. To support IGMPv3/MLDv2, a SIP entry is added to search the Source IP list after DIP look-up.

2.5.1 MAC Address Table

MAC Address Table

Bytes	Bits	Name	Description
7:0	11:0	CVID	Customer VID [11:0] Customer VLAN ID is learned automatically from VLAN tag or port-based register PPBV# .PORT_VID.
	14:12	FID	Filter ID[2:0] Filter ID is learned automatically from VLAN Table. 0 is the default value if VLAN Table is not applicable.
	15	IVL	Independent VID Learning IVL is learned automatically from VLAN Table. 0 is the default value if VLAN Table is not applicable.
	63:16	ADDRESS	MAC Address[47:0] 48-bits MAC Physical Address is searched by Destination MAC Address and learned from Source MAC Address.
Bytes	Bits	Name	Description
3:0	1:0	TYPE	Layer2/Layer3 Address Entry Type 2'b00: MAC Address Entry 2'b01: DIP Address Entry. 2'b10: Source IP Address Table 2'b11: Reserved
	3:2	STATUS	Address Entry Live Status 2'b00: Entry is empty 2'b01: Entry is dynamic and valid 2'b10: Reserved 2'b11: Entry is static and won't be aged out or changed by the hardware
	11:4	PORT / FILTER	Destination Port Map (Note: Frame dropped by DA Address through PORT=6'b0) Bit4: Port 0 ~ Bit11: Port 7
	12	LEAKY_EN	Leaky VLAN Enable 1'b0: This frame address will be blocked by VLAN (default) 1'b1: This frame address can pass through VLAN

			(Note: Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MFC.UC_ARL_LKYV or MFC.MC_ARL_LKYV.)
15:13	EG_TAG		Egress VLAN Tag Attribution 3'b000: System default (Default) 3'b001: Consistent 3'b010,3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
18:16	USR_PRI		User Priority from Address Table 0: Default
19	SA_MIR_EN		Source Address Hit to Mirror port 1'b0: No action (default) 1'b1: Frame is copied to mirror port when SA hits the MAC table
22:20	SA_PORT_FW		Source Address Hit Frame TO_CPU Forwarding 3'b0xx: System Default (Disable) 3'b100: System Default and CPU Port Excluded 3'b101: System Default and CPU Port Included 3'b110: CPU Port Only (while the ingress port is not CPU port, otherwise system default and CPU excluded) 3'b111: Frame Dropped
23	-		Reserved
31:24	TIMER		Age Timer Programmable age timer. The age duration can be set from 1 to 1,000,000 seconds. The field value will be reset to the register AAC.AGE_CNT and counted down by one every AAC.AGE_UNIT seconds.

2.5.2 Destination IP Address Table

While receiving IP Multicast frames, the destination IP will be used to search the address table. For this usage, the address entry has TYPE=2'b01 (IGMPv2). The table is shown below.

DIP Address Table

Bytes	Bits	Name	Description
7:0	15:0	RESP_CNT	Response Counter[15:0] A response counter for each port is used to count the consecutive occurrence times of no IGMP Report message received before the Response Timer counts to zero. Bit[49:48]: Port 0 ~ Bit[63:62]: Port 7
	23:16	RESP_FLAG	Response Flag[7:0]

			After receiving the Group Query or Group Specific Query, this flag is used to record any IGMP report message received for the corresponding port before the response interval counts to zero. Bit40: Port 0 ~ Bit47: Port 7
	31:24	RESP_TIMER	Response Timer[7:0] This timer will be set according to the maximum response time field in the General Specific Query message and count down every second. The default timer for the General Query message (=0x0) is 10 seconds.
	63:32	ADDRESS	IP Multicast Destination IP Address[31:0] The latest 32-bits DIP(GA) for IPv4 or IPv6 packets
Bytes	Bits	Name	Description
3:0	1:0	TYPE	Layer2/Layer3 Address Entry Type 2'b00: MAC Address Entry 2'b01: DIP Address Entry 2'b10: Source IP Address Table 2'b11: Reserved
	3:2	STATUS	Address Entry Live Status 2'b00: Group entry is empty. 2'b01: Group entry is dynamically valid whenever any IGMP report message received before the response timer counts to zero, and the response counter is not larger than the robustness variable. 2'b10: Entry is static, and the final port map will result from the SIP table search. 2'b11: Entry is static and will not be aged out or changed by the hardware.
	11:4	PORT / FILTER	Destination Port Map or Filter Mode for IGMPv3/MLDv2 Bit4: Port 0 ~ Bit11: Port 7
	12	LEAKY_EN	Leaky VLAN Enable 1'b0: This frame address will be blocked by VLAN (default). 1'b1: This frame address can pass through VLAN. (Note: Leaky VLAN can be configured by ARL or Port Control Register based on the indication of MFC.UC_ARL_LKYV or MFC.MC_ARL_LKYV.)
	15:13	EG_TAG	Egress VLAN Tag Attribution 3'b000: System default (Default) 3'b001: Consistent 3'b010 ~ 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
	18:16	USR_PRI	User Priority from IGMP Table 0: Default

	31:19	-	Reserved

2.5.3 Source IP Address Table

The internal 2K entries address table can also be used for Source IP table for IGMPv3. For this usage, the address entry has TYPE=2'b11. The table is shown below.

Source IP Address Table

Bytes	Bits	Name	Description
7:0	31:0	SIP_ADR	IP Multicast Source IP Address [31:0] The latest 32-bits IPv4 or IPv6 Source address
	63:32	DIP_ADR	IP Multicast Destination IP Address [31:0] The latest 32-bits IPv4 or IPv6 Destination or Group address
Bytes	Bits	Name	Description
3:0	1:0	TYPE	Layer2/Layer3 Address Entry Type 2'b00: MAC Address Entry 2'b01: DIP Address Entry 2'b10: Source IP Address Table 2'b11: Reserved
	3:2	STATUS	Address Entry Live Status 2'b00: Group entry is empty 2'b01 ~ 10: Reserved 2'b11: Entry is static and won't be aged out or changed by the hardware
	11:4	PORT_MAP	Port Member Bit.4: Port 0 ~ Bit.1: Port 7
	31:12	-	Reserved

2.6 Virtual LAN

2.6.1 VLAN Table

VLAN Table

Bits	Name	Description
0	VALID	VLAN Entry Valid
3:1	FID	Filtering Database 3'h0: Default FID for all MAC address ~ 3'h7
15:4	S_TAG1	(1) Service Tag Identification (VLAN Table PORT_STAG=1'b0) 12-bits Service Tag ID for VLAN translation or Stack VLAN (2) Service Tag Index (VLAN Table PORT_STAG=1'b1) bit[5:4]: Port 0 STAG index bit[7:6]: Port 1 STAG index bit[9:8]: Port 2 STAG index bit[11:10]: Port 3 STAG index bit[13:12]: Port 4 STAG index bit[15:14]: Port 5 STAG index
23:16	PORT_MEM	VLAN Member Control (Note: Frame dropped through PORT=6'b0) Port 0 - Bit 0: VID Port Member ~ Port 7 - Bit 7: VID Port Member
26:24	USER_PRI	Service Tag User Priority Value from VLAN Table
27	COPY_PRI	Copy User Priority Value from Customer Priority Tag for Stack VLAN
28	VTAG_EN	Per VLAN Egress Tag Control Enable per-vlan egress tag attribute by EG_CON and EG_TAG
29	EG_CON	Egress Tag Consistent Keep the original ingress tag attribute. (Note: When the EG_CON is set, EG_TAG will be invalid for the outgoing frames)
30	IVL_MAC	MAC Address Learned by Individual CVID 1'b0: MAC address will be learned by MAC and FID 1'b1: MAC address will be learned by MAC and CVID
31	PORT_STAG	Port-based STAG 1'b0: S_TAG1 shows 12-bit VID 1'b1: S_TAG1 and S_TAG2 show 2-bit STAG index on per port.
47:32	EG_TAG	VLAN Egress Tag Control Bit.33~Bit.32 (Port 0) – 2'b00: Untagged 2'b01: Swap

		2'b10: Tagged 2'b11: Stack ~ Bit.47 ~ Bit.46 (Port 7)
59:48	S_TAG2	(2) Service Tag Index bit[49:48]: Port 6 STAG index bit[51:50]: Port 7 STAG index bit[59:52]: Reserved

2.6.2 VLAN Security Mechanism

The ingress port can support VLAN security or flexible ingress rule. There are four ingress port attributes described as follows -

2'b11: Security mode

Enable 802.1Q VLAN for all the received frames.

Discard received frame due to ingress membership violation (interrupt CPU).

Discard received frames once if VID is missed on the VLAN table (interrupt CPU).

2'b10: Check mode

Enable 802.1Q function for all the received frames.

Do not discard received frame due to ingress membership violation.

Discard received frames once if VID is missed on the VLAN table (interrupt CPU).

2'b01: Fallback mode

Enable 802.1Q function for all the received frames.

Do not discard received frame due to ingress membership violation.

Frames whose VID is missed on the VLAN table will be filtered by the Port Matrix Member.

2'b00: Port Matrix mode

802.1Q function is disabled (VLAN Security and VLAN Filter Table).

Frames filtered by the Port Matrix Member

2.6.3 VLAN Membership Resolution

VLAN Membership Resolution

ACL	PCR.PORT_VLAN	VLAN	VLAN Member	Action
Hit	-	-	-	Use Port in Rule Control Table
Not Hit	Port Matrix	-	-	Use PORT_MATRIX in PCR register
	Fallback	Hit	-	Use PORT_MATRIX(PCR) & PORT_MEM(VLAN Table)
		Not Hit	-	Use PORT_MATRIX in PCR register
	Check	Hit	-	Use PORT_MATRIX(PCR) & PORT_MEM(VLAN Table)
		Not Hit	-	Frame Dropped
	Security	Hit	Yes	Use PORT_MATRIX(PCR) & PORT_MEM(VLAN Table)

		-	-	Frame Dropped

2.6.4 VLAN Tagging

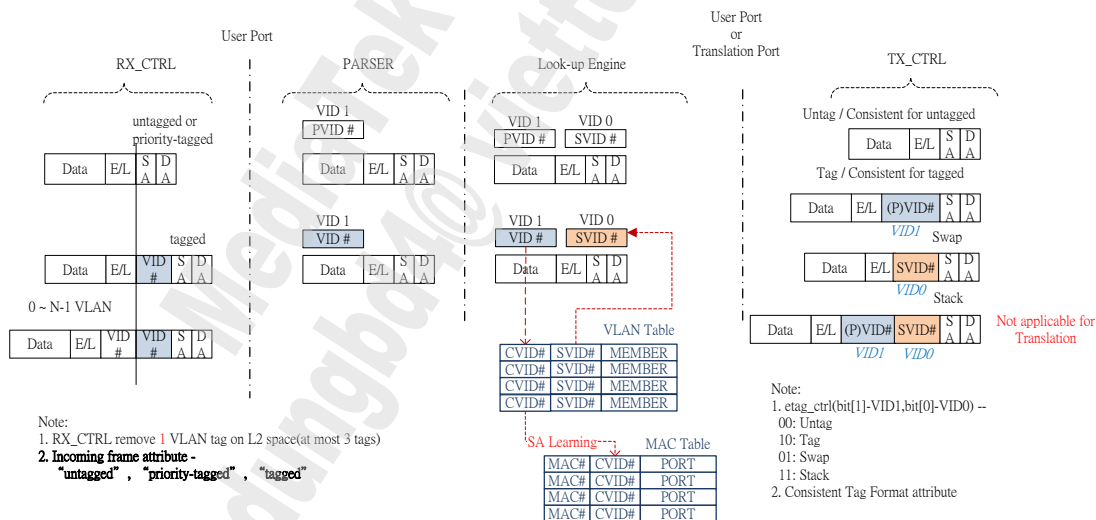
The switch can support customer and service VLAN tags (inner/ outer VLAN tags) inside a frame. When a frame is incoming, its VLAN tags will be stripped by one or two based on different ingress port attributes – PVC.VLAN_ATTR. Similarly, their tags will be used for VLAN table search or MAC table search according to the incoming port attribute.

Finally, the per-port egress tag control will be carried on the TX_CTRL side. The transmitted frame will follow the egress control and carry the processed VLAN tags - VID0 (service tag) and VID1 (customer tag).

2.6.4.1 User port

The incoming VLAN-tagged frame is stripped by the outer tag despite the following inner tags. Per untagged or priority-tagged frame, PVID is treated as VID1 tag. At the same time, VID1 is used to look for VLAN table to get the FID and Service tag for VID0. When a new Source MAC address is learned, the VID1 will also be learned on the MAC table.

On the TX_CTRL side, each frame carries 2*N-port egress control bits on per-port based. Bit0 indicates whether this frame carries VID 0 or not; similarly, Bit.1 is for VID1. Once "Consistent tag" is set, the egress tag format will follow the ingress tag format.

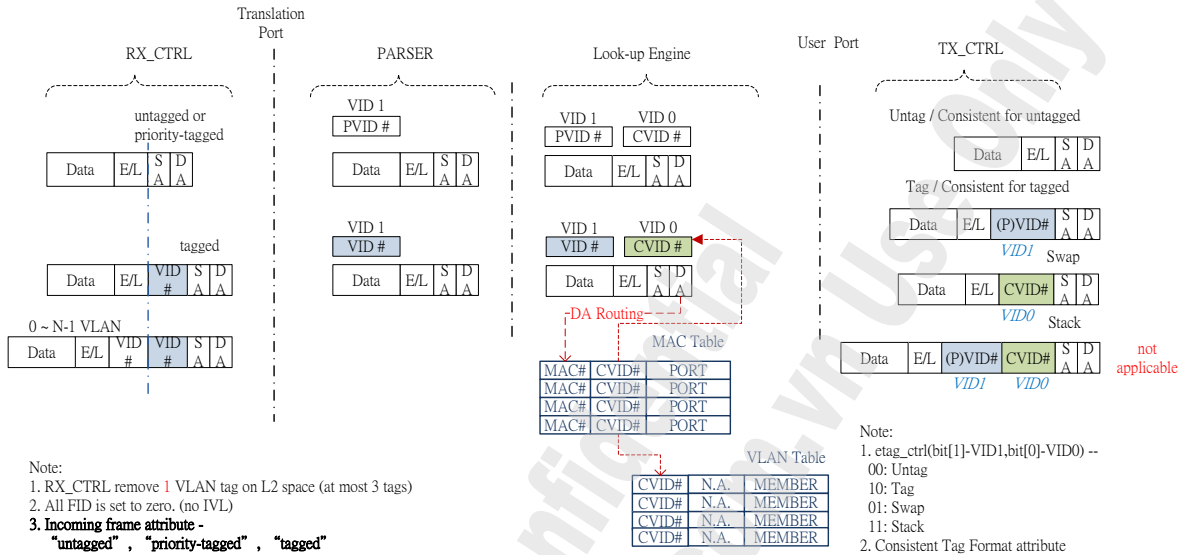


VLAN Tag Process on User Port

2.6.4.2 Translation port

The translation port is designated for 1:1 or N:1 VLAN aggregation according to CHINA TELECOM EPON requirement. When an incoming frame is received on the translation port, the corresponding custom VID will be found from MAC table, and then the CVID will be the VID for VLAN table.

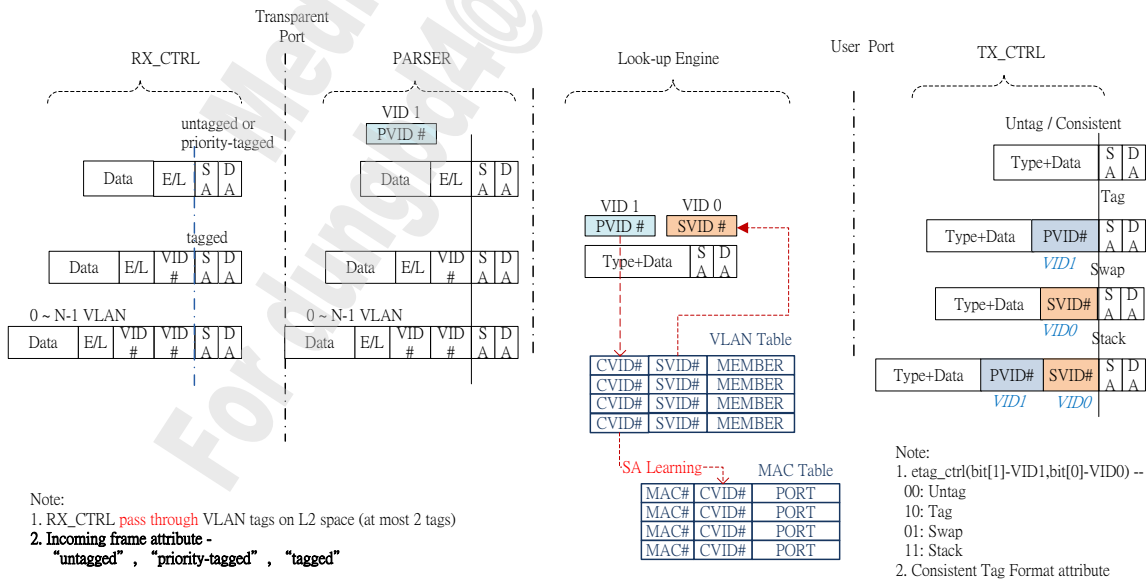
In the uploading direction, several custom VIDs can be translated into one service VID from the VLAN table which is carried on VID0. When this frame is transmitted from the translation port, etag_ctrl[1:0] will be 2'b01 (Swap), and the service VID will appear on the egress frame.



VLAN Tag Process on Translation Port

2.6.4.3 Transparent port

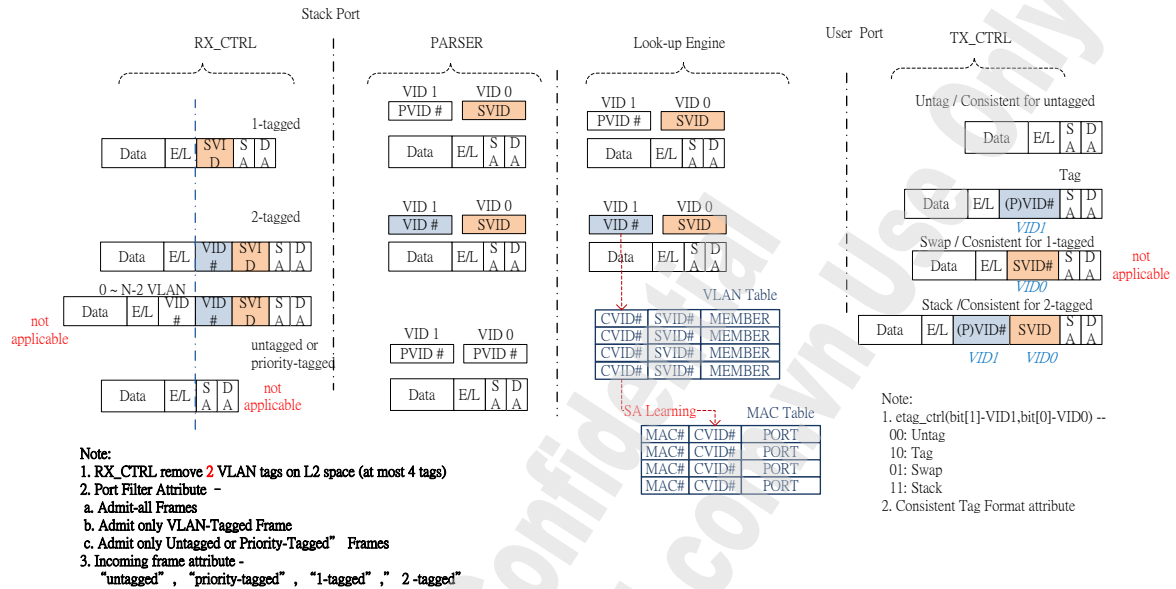
When the port is chosen as transparent port, the VLAN tags on the incoming will be ignored and treated as untagged frames. VID0 and VID1 will store PVID as the default VID which is used to look up the VLAN table. On the egress side, TX_CTRL can accept "UNTAG" control to send the original frame.



VLAN Tag Process on Transparent Port

2.6.4.4 Stack port

For stack port, the incoming frames should carry at least one service VID on the outer tag. The outer tag will be stripped on the received port and saved on VID0. If there is a second tag, the CVID will be saved on VID1 and used for VLAN table look-up. Otherwise, PVID will replace CVID and will be saved on VID1.



VLAN Tag Process on Stack Port

2.6.5 Egress VLAN Tag Process

EG_TAG Attribute Priority Resolution

ACL	FTAG	ARL	PVC.EG_TAG	VLAN	Action
Hit	-	-	-	-	Use EG_TAG in Rule Control Table
Not Hit	PPPoE	-	-	-	Use EG_TAG in APC register
	Discovery	-	-	-	
	ARP/RARP	-	-	-	
	IGMP/MLD	-	-	-	Use EG_TAG in IMC register
	BPDU and PAE	-	-	-	Use EG_TAG in BPC register
	REV_01, REV_02, REV_03, REV_0E, REV_10, REV_20, REV_21, REV_UN	-	-	-	Use EG_TAG in RGAC1~ RGAC4 registers
	Other	Hit	-	-	Use EG_TAG in Address Table

		Not Hit	Hit	-	Use EG_TAG in PVC register
			Not Hit	Hit	Use EG_CON and EG_TAG in VLAN Table
				Not Hit	Use EG_TAG in PCR register

2.6.6 Special Tag

In order to notify the link partner of the incoming port number of a received frame, a special tag is used to rewrite the TPID (0x8100) field. The format of this rewritten TPID on egress direction (TX) is shown below. To enable this feature, user can enable the specific egress ports that need incoming port number to be carried by TPID by setting associated ports in P#_PVC.PORT_STAG. Note that this special tag feature is a supplement to the existing VLAN tag feature. If the egress frame does not have VLAN tag, there is no way to put incoming port number into the modified TPID field. If the egress frame is double VLAN tagged, the special tag applies to the outer VLNA tag only.

On the opposite receiving direction, ARL can recognize the incoming outer tag which carries the special tag format (RX) and has the proprietary control or resolution on forwarding port, user priority and so on. This is additional in-band control information when switch is used as the company chip to upper SoC or NAT engine.

Rx:		FUP		UPRI[2:0]		DVP		DRM		VPM[1:0]	
		PT		SA		DP[5:0]					
Tx:		0		0		0		0		VPM[1:0]	
		PT		0		0		0		SPN[2:0]	

Signals	width	Descriptions
PT	1	Pass Through
DP[5:0]	5	Force forwarding port map; all 0 means disable
SA	1	Disable SA learning
VPM	2	Tag attribute before special tag insertion; 2'b00: untagged, 2'b01: TPID=8100, 2'b10: TPID=predefined (e.g. 0x9100 or 0x88a8)
FUP	1	Force PPE User Priority
UPRI[2:0]	3	PPE User Priority
DRM	1	Disable DSCP priority remarking
DVP	1	Disable VLAN priority remarking
SPN[2:0]	3	source port no.

Special Tag Format

2.7 Spanning Tree Protocol

2.7.1 Port State

When using IEEE 802.1D, the ARL supports eight FID and four Port States on CSR - SSC for each port for CPU implementation 802.1D (STP/RSTP) and 802.1s (MSTP) functions as shown in the following table.

IEEE 802.1D Port State

STP	RSTP	RX/TX BDPU	LEARN Address	RX User Frames	TX User Frames
Disabled	Discarding	--	--	--	--
Blocking/Listening	Discarding	V	--	--	--
Learning	Learning	V	V	V	--
Forwarding	Forwarding	V	V	V	V

- **Disabled:**

The port will not transmit/receive any packet.

- **Blocking/Listening:**

The port will receive and transmit BPDU spanning tree protocol packets but will not transmit any user packet nor perform learning.

- **Learning:**

The port will receive any packet, including BPDU spanning tree protocol packets and will perform learning, but it will only transmit BPDU spanning tree protocol packets.

- **Forwarding:**

The port will receive and transmit all packets, and it will also perform learning.

2.7.2 Rapid Spanning Tree Protocol

RSTP is the IEEE 802.1w amendment to the 802.1D standard for improving the performance. The Rapid Spanning Tree Protocol (RSTP) is a transformation of the Spanning Tree Protocol, which is implemented in most LANs today.

- **Discarding:**

The STP port states of listening, blocking, and disabled have been combined in RSTP to the state of discarding.

- **Learning:**

The port is preparing to forward data traffic. Because the port's address table may be empty, it is generally not a good idea to begin forwarding data traffic yet.

- **Forwarding:**

Once the bridge has spent some time learning addresses, it is allowed to forward data frames.

2.7.3 Multiple Spanning Tree Protocol

The Multiple Spanning Tree Protocol (MSTP) is originally defined in IEEE 802.1s and is later merged into IEEE802.1Q. It is an extension of the RSTP protocol which allows independent configuration as a separated spanning tree for each VLAN group.

2.8 Access Control Logic (ACL)

Although Ethernet switch or bridge is well-defined by IEEE Std.802.3, additional requirements are still needed for it to fit in future standards or to improve security, QoS, or policy control. ARL provides 256 entries ACL rule table and 128 entries ACL rule control table with wire-speed on the incoming frames.

2.8.1 ACL Rule Table

ACL rule table is implemented along with packet parser. For the incoming packet, the 2-bytes packet content is filtered sequentially and compared with 256 patterns in the ACL rule table. When one pattern is hit, the corresponding rule flag will be set. After the whole packet is done, the final rule flag will be sent to the ACL look-up engine to get the corresponding rule control.

ACL Rule Table

Byte	Bit	Name	Description
1:0	15:0	CMP_PAT	Comparison Pattern If CMP_SEL=='b0, this field indicates the 16-bits data pattern. If CMP_SEL=='b1, this field indicates the low threshold.
3:2	15:0	BIT_CMP	Comparison Pattern Mask If CMP_SEL=='b0, this field indicates the bit-map valid comparison. If CMP_SEL=='b1, this field indicates the high threshold.
4	0	CMP_SEL	Comparison mode selection 'b0: Pattern hit by data pattern and bit mask 'b1: Pattern hit by low and high threshold
	7:1	WORD_OFST	Word Offset 2-bytes offset in the corresponding OFST_TP. (Note: 0x3F is the reserved and invalid offset value.)
5	7:0	SP	Physical Source Port Bit-map SP[7:0]: port 7 ~ port 0
6	2:0	OFST_TP	Format Type for Word Offset Range 3'b000: MAC Header (inc. VLAN tags and Length/Type) (L2 Offset) 3'b001: L2 Payload (L2 Offset) 3'b010: IP Header (L3 Offset) 3'b011: IP Datagram (L3 Offset) 3'b100: TCP/UDP Header (L4 Offset) 3'b101: TCP/UDP Datagram (L4 Offset) 3'b110: IPv6 Header (L3 Offset) 3'b111: Reserved
	3	EN	ACL Valid Bit

2.8.2 ACL Rule Control Table

ACL rule control is a 128 entries table with a linear look-up engine. Each packet can find one or multiple hit entries from the ACL rule control. For the general packet control, the first hit entry will be taken and followed during the packet process. As for the ACL rate limit control, multiple entries can be applied on the same packet.

ACL Rule Mask

Byte	Bit	Name	Description
15:0	127:0	HIT_PAT	Hit Pattern - When a valid bit is set in this table, it means that the corresponding pattern in the rule table must be hit and necessary. If all the valid bits can be found in the rule flag, then the rule control can be applied on this packet.

ACL Rule Control Table

Byte	Bit	Name	Description
0	2:0	PORT_FW	Frame TO_CPU Forwarding 3'b0xx: System Default (Disable) 3'b100: System Default and CPU Port Excluded 3'b101: System Default and CPU Port Included 3'b110: CPU Port Only (When the ingress port is not a CPU port it will follow, the system default and CPU are excluded) 3'b111: Frame Dropped
	3	MIR_EN	Frame Copy to Mirror Port
	6:4	PRI_USER	User Priority from ACL
	7	PORT_EN	Force Destination Port Selection 1'b0: Destination port is based on ARL or register 1'b1: Destination port is based on PORT.
1	7:0	PORT	Destination Port Member / VLAN Port Member
2	2:0	EG_TAG	Egress VLAN Tag Attribution 3'b000: System Default (Disable) 3'b001: Consistent 3'b010,3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
	3	LKY_VLAN	Leaky VLAN
	4	PPP_RM	PPPoE Header Removal
	5	SA_SWAP	Source MAC Address Swap

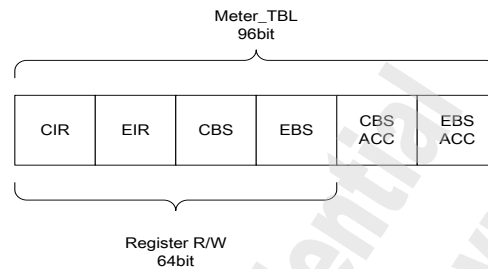
	6	DA_SWAP	Multicast MAC Destination Address Swap IPv4: 01-00-5E-xx-xx-xx (From Destination IP) IPv6: 33-33-xx-xx-xx-xx (From Destination IP)
	7	VLAN_PORT_EN	Swap VLAN Port Member with PORT
3 (Counter)	2:0	CNT_IDX	Counter Group Index
	3	ACL_CNT_EN	Enable ACL Hit Count (Multi/First)
	4	INT_EN	Interrupt Enable (Multi/First)
	5	ACL_MANG	Management Frame Attribute
	7:6	-	Reserved
6:4 (trTCM)	0	DROP_PCD_SEL	Select original drop precedence value or ACL control table defined drop precedence value
	1	CLASS_SLR_SEL	Select original class_selector value or ACL control table defined class selector value
	4:2	CLASS_SLR	User defined class selector
	7:5	DROP_PCD_R	User defined drop precedence value for red color packet
	2:0	DROP_PCD_Y	User defined drop precedence value for yellow color packet
	5:3	DROP_PCD_G	User defined drop precedence value for green color packet
	7:6	--	Reserved
	0	ACL_TCM_SEL	Select color remark by Meter Table or use defined color value
	2:1	ACL_TCM	User defined color remark (00: Default, 01: Green, 10: Yellow, 11: Red)
	7:3	ACL_CLASS_IDX	Class index for the 32-entries Meter Table

ACL Rate Control

Byte	Bit	Name	Description
1:0	13:0	RATE	Per Flow Ingress Rate Limit Control Per rate limit, multiple rule controls can constraint one packet. Generally, the minimum ingress rate limits the flow rate. 14'h0: 0 * 64Kbps or 1Mbps (according to CR 0xC[30]) 14'h1: 1 * 64Kbps or 1Mbps 14'h2: 2 * 64Kbps or 1Mbps ~~ 14'h3D09: 15625 * 64Kbps or 1Mbps
	14	MANG_EN	Per Flow for Management Frame Ingress Rate Control Enable
	15	RATE_EN	Per Flow Ingress Rate Limit Enable (Multi/First)
3:2	14:0	RATE_ACCU	Per Flow Ingress Rate Limit Accumulator
	15	-	Reserved

2.9 Two-Rate Three Color Marker (trTCM)

The trTCM engine supports 32 entries of metering table. Each service is entitled as independent committed information rate (CIR), peak information rate (EIR), committed burst size (CBS) and peak burst size (EBS). These metering criteria are used to assign different colors for each incoming packet. The meter table can be read/write from the register for CIR/PIR/CBS/PBS. When the table is written, the CBS_ACC and PBS_ACC are filled zero. This means that the buckets for C and P are empty initially.



trTCM Meter-Table

Bits	Type	Name	Description	Initial value
63:48	RW	CIR	Committed Information Rate 16'h0: 0 * 64Kbps 16'h1: 1 * 64Kbps ~~~~ 16'hFFFF: 65536 * 64Kbps (Note: 1*64Kbps means that ACL will add 1 token (1-Byte) to the CBS burst bucket every 125us.)	0x0
47:32	RW	PIR	Peak Information Rate 16'h0: 0 * 64Kbps 16'h1: 1 * 64Kbps ~~~~ 16'hFFFF: 65536 * 64Kbps (Note: 1*64Kbps means that ACL will add 1 token (1-Byte) to the PBS burst bucket every 125us.)	0x0
31:16	RW	CBS	Committed Burst Size The maximum number of bytes allowed for incoming packets to burst above the CIR, but the incoming packets are still marked green. The CBS burst size should be larger than CIR for the token added.	0x0
15:0	RW	PBS	Peak Burst Size The maximum number of bytes allowed for incoming packets to burst above the CIR, and they are still marked yellow. The PBS burst size should be larger than PIR for token added.	0x0

2.10 Register Definition

2.10.1 ARL Register

Module name: ARL Base address: (+0x0000)

Address	Name	Width	Register Function
00000004	<u>CFC</u>	32	CPU Forward Control
00000008	<u>AISR</u>	32	ACL Interrupt Status
0000000C	<u>AGC</u>	32	ARL Global Control
00000010	<u>MFC</u>	32	MAC Forward Control
00000014	<u>VTC</u>	32	VLAN TAG Control
00000018	<u>ISC</u>	32	IGMP Snooping Control
0000001C	<u>IMC</u>	32	IGMP/MLD Message Control
00000020	<u>APC</u>	32	ARP and PPPoE Control
00000024	<u>BPC</u>	32	BPDU and PAE Control
00000028	<u>RGAC1</u>	32	REV_01 and REV_02 Control
0000002C	<u>RGAC2</u>	32	REV_03 and REV_0E Control
00000030	<u>RGAC3</u>	32	REV_10 and REV_20 Control
00000034	<u>RGAC4</u>	32	REV_21 and REV_UN Control
00000038	<u>PMC</u>	32	Protocol Match Control
0000003C	<u>PBG1</u>	32	Protocol Based Group ID-1
00000040	<u>PBG2</u>	32	Protocol Based Group ID-2
00000058	<u>PIM1</u>	32	DSCP Priority Ingress Mapping I
0000005C	<u>PIM2</u>	32	DSCP Priority Ingress Mapping II
00000060	<u>PIM3</u>	32	DSCP Priority Ingress Mapping III
00000064	<u>PIM4</u>	32	DSCP Priority Ingress Mapping IV
00000068	<u>PIM5</u>	32	DSCP Priority Ingress Mapping V
0000006C	<u>PIM6</u>	32	DSCP Priority Ingress Mapping VI
00000070	<u>PIM7</u>	32	DSCP Priority Ingress Mapping VII
00000074	<u>ATA1</u>	32	Address Table Access I
00000078	<u>ATA2</u>	32	Address Table Access II
0000007C	<u>ATWD</u>	32	Address Table Write Data
00000080	<u>ATC</u>	32	Address Table Control
00000084	<u>TSRA1</u>	32	Table Search Read Address I
00000088	<u>TSRA2</u>	32	Table Search Read Address II
0000008C	<u>ATRD</u>	32	Address Table Read Data
00000090	<u>VTCR</u>	32	VLAN Table Control
00000094	<u>VAWD1</u>	32	VLAN and ACL Write Data I
00000098	<u>VAWD2</u>	32	VLAN and ACL Write Data II
0000009C	<u>TRTCM</u>	32	Two Rate Three Color Mark
000000A0	<u>AAC</u>	32	Address Age Control
000000A4	<u>DHCP</u>	32	DHCP Control
000000A8	<u>LCP</u>	32	PPPoE LCP Control
000000AC	<u>MHS</u>	32	MAC Table Hash Seed
000000B0	<u>CPGC</u>	32	Collision Pool Global Control
000000B4	<u>CPMONC</u>	32	Collision Pool Monitor Control
000000B8	<u>CPMOND1</u>	32	Collision Pool Entry Status Monitor 1
000000BC	<u>CPMOND2</u>	32	Collision Pool Entry Status Monitor 2
000000C0	<u>CPSTSC</u>	32	Collision Pool Status Counter
000000C4	<u>AISR_EXT1</u>	32	ACL Extension Interrupt Status I

000000C8	<u>AISR_EXT2</u>	32	ACL Extension Interrupt Status II
000000CC	<u>AISR_EXT3</u>	32	ACL Extension Interrupt Status III
000000D0	<u>MISR</u>	32	MLDv2 Interrupt Status
000000D4	<u>MISR_EXT1</u>	32	MLDv2 Extension Interrupt Status I
000000E0	<u>VAWD3</u>	32	ACL Write Data III
000000E4	<u>VAWD4</u>	32	ACL Write Data IV
000000E8	<u>VAWD5</u>	32	ACL Write Data V
000000EC	<u>VAWD6</u>	32	ACL Write Data VI
000000F0	<u>VAWD7</u>	32	ACL Write Data VII
000000F4	<u>VAWD8</u>	32	ACL Write Data VIII
00000100	<u>PTC</u>	32	Port Trunking Control
00000104	<u>PTHS</u>	32	Port Trunking Algorithm Seed
00000108	<u>PTGC0</u>	32	Port Trunking Group Control 0
0000010C	<u>PTGC1</u>	32	Port Trunking Group Control 1
00000110	<u>PTGC2</u>	32	Port Trunking Group Control 2
00000114	<u>PTGSC0</u>	32	Port Trunking Group Security Control 0
00000118	<u>PTGSC1</u>	32	Port Trunking Group Security Control 1
0000011C	<u>PTGSC2</u>	32	Port Trunking Group Security Control 2
00000120	<u>SPTC0</u>	32	Port Trunking Table Control

00000004 CFC CPU Forward Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												MIRRO R_EN	MIRROR_PORT		
Type	RW												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1								CPU_PMAP							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	Reserved
19	MIRROR_EN	Mirror Port Enable Enable the mirror port specified in MIRROR_PORT. 0: No mirror available 1: Enable mirror
18:16	MIRROR_PORT	Mirror Port Number Set the mirror port number. 3'h0: Port 0 ... 3'h7: Port 7
15:8	REV1	Reserved
7:0	CPU_PMAP	CPU Port Bit Map Provide multiple CPU port selection. [0]: Port 0 [1]: Port 1 ... [7]: Port 7

00000008 AISR ACL Interrupt Status 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_ISR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACL_ISR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ACL_ISR	ACL Interrupt Status for entry 0~31 (Refer to ACL Rule Control Table)

0000000C AGC ARL Global Control 0007181D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MLDv2_int_en	TICK_SEL	PCP_AWARE	SNOP_DROP	REV0			MAC_SARLP_DIS	REV1		MAC_HASH_SE_L		REV2	ACL_INT	VLAN_INT	ADDR_INT
Type	RW	RW	RW	RW	RO			RW	RO		RW		RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RATE_COMP	COMP_BNUM							LOCAL_EN	ARL_P_ADDING	ACL_MULT	L2LEN_CHK	CTRL_DROP	VLAN4_CPU	ARL_PRIORITY	ALR_RST_N
Type	RW	RW							RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	1	1	0	0	0	0	0	0	1	1	1	0	1

Bit(s)	Name	Description
31	MLDv2_int_en	MLDv2 interrupt enable 0: Disable 1: Enable
30	TICK_SEL	Select 64Kbps or 1Mbps tick in ACL rate control for supporting 2.5G rate limit 0: 64Kbps tick 1: 1Mbps tick
29	PCP_AWARE	Priority-tag aware for dump switch 0: Disable priority-tag 1: Enable priority-tag
28	SNOP_DROP	IGMP snooping can learn the dropped frame 0: IGMP snoop will ignore the dropped frame 1: IGMP snoop will learn the dropped frame
27:25	REV0	Reserved
24	MAC_SARLP_DIS	Disable oldest address replacement function for mac address learning. In default, oldest mac address will be replaced by new address when there are no empty entry for mac address learning Manual update address table won't be affected 0: Replace oldest mac address 1: Not to replace oldest mac address
23:22	REV1	Reserved

Bit(s)	Name	Description
21:20	MAC_HASH_SEL	Select MAC Table Hash Function 2'b00: XOR 2'b01: CRC16 2'b10: CRC32
19	REV2	Reserved
18	ACL_INT	Access Control List (ACL) Table Initialization Done 0: ACL Table is busy. 1: ACL Table is cleared.
17	VLAN_INT	VLAN Table Initialization Done 0: VLAN Table is busy. 1: VLAN Table is cleaned.
16	ADDR_INT	ADDR Table Initialization Done 0: ADDR Table is busy. 1: ADDR Table is cleaned.
15	RATE_COMP	Rate Limit Compensation Add or subtract the specific byte number while calculating the packet length. 0: Add 1: Minus
14:8	COMP_BNUM	Compensation Byte Number The added/subtracted byte number for the rate limit or the meter table
7	LOCAL_EN	Local Port Forwarding Enable 0: Drop frames at the local port. 1: Allow frame forwarding to the local port.
6	ARL_PADDING	ARL Data Padding Set ARL to add byte padding up to 46 bytes when the length of the data field of the incoming frame is less than 46 bytes. 0: Disable (default) 1: Enable
5	ACL_MULTI	Enable Multiple ACL Hit 0: Only the first hit ACL entry 1: Allow multiple ACL hit entries on Rate, Interrupt, and MIB.
4	L2LEN_CHK	Layer 2 Frame Length Check Enable a length check on length-encapsulated frame. Drop length error frames when the value of the ELEN field of this frame is bigger than the length of the data field. 0: Disable 1: Enable
3	CTRL_DROP	MAC Control Frame Drop Drop MAC control frames with ETYPE=0x8808. 0: Disable (default) 1: Enable
2	VLAN4CPU	TO_CPU VLAN Member Set the TO_CPU frame to check VLAN members. 0: Ignore VLAN members. 1: Check VLAN members.
1	ARL_PRI	ARL Resolution Priority 0: P0 is the lowest priority. 1: P0 is the highest priority.
0	ALR_RST_N	ARL Enable (Soft Reset) 0: Reset the ARL engine. 1: Enable ARL engine.

00000010 MFC MAC Forward Control FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BC_FFP								UNM_FFP							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UNU_FFP								QRY_FFP							
Type	RW								RW							
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	BC_FFP	Broadcast Frame Flooding Ports If MAC receives broadcast frames, this field indicates the flooding ports. [NOTE] 1. The flooding port excludes the received port on the switch. 2. Frame dropped though BC_FFP=7'b0
23:16	UNM_FFP	Unknown Multicast Frame Flooding Ports If MAC receives multicast frames which can not be found on the ARL, this field indicates the flooding ports. [NOTE] 1. The flooding port will exclude the received port by HW. 2. Frame dropped though UNM_FFP=7'b0.
15:8	UNU_FFP	Unknown Unicast Frame Flooding Ports If MAC receives the unicast or multicast frames which can not be found on the ARL. The field indicates the flooding port. [NOTE] 1. The flooding port will excludes the received port by HW 2. Frame dropped though UNM_FFP=7'b0
7:0	QRY_FFP	IGMP/MLD Query Frame Flooding Ports If MAC receives IGMP/MLD query frame, this field indicates the flooding ports. [NOTE] 1. The flooding port will exclude the received port by HW. 2. Frame dropped though QRY_FFP=7'b0.

00000014 VTC VLAN TAG Control 000000FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													REVO			
Type													RW			
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO								GUEST_MEM							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
19:8	REVO	Reserved
7:0	GUEST_MEM	Guest VLAN Member The assigned VLAN member for the frames which cannot pass 802.1x authentication

00000018 ISC IGMP Snooping Control 7F027DFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	LRN_RP								REV0			DWN_GRADE_EN	MLD_RP_EN	IGMP_RP_EN	ROBUST_VAR	
Type	RO								RW			RW	RW	RW	RW	
Reset	0	1	1	1	1	1	1	1	0	0	0	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	QRY_INTL								DEF_RP							
Type	RW								RW							
Reset	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:24	LRN_RP	Learned Router Ports Show the router ports for IGMP/MDL messages including the default and learned ports.
23:21	REV0	Reserved
20	DWN_GRADE_EN	IGMP v2 to v1 Auto-Downgrade Enable Enable an automatic downgrade from IGMPv2 to v1 due to a IGMPv1 report message. 0: Disable 1: Enable
19	MLD_RP_EN	MLD Router Port Learning Enable Enable automatic router port learning automatically based on MLD queries. 0: Disable 1: Enable
18	IGMP_RP_EN	IGMP Router Port Learning Enable automatic router port learning based on IGMP queries. 0: Disable 1: Enable
17:16	ROBUST_VAR	Robustness Variable Define the maximum allowable number of IGMP Query messages that may be lost consecutively. 0: Reserved 1: One time 2: Two times (default) 3: Three times
15:8	QRY_INTL	Query Interval Together with the Robustness Variable, the Query Interval sets the age-out time for router ports automatically learned from IGMP Query frames. Age-out time = (QRY_INTL * ROBUST_VAR) (unit: sec)
7:0	DEF_RP	Default Router Port Set the default router port which will not be aged out when IGMP/MLD router port learning is enabled.

0000001C IMC IGMP/MLD Message Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MDL_RPT_MIR	MLD_RPT_FW				MLD_MANG_FR	MLD_PAE_FR	MLD_BPDU_FR	MLD_EG_TAG			MLD_LKY_VLAN	MLD_PRI_HIGH	MLD_QUE_MIR	MLD_QUE_FW		
Type	RW	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	IGMP_RPT_MIR	IGMP_RPT_FW				IGMP_MANG_FR	IGMP_PAE_FR	IGMP_BPDU_FR	IGMP_EG_TAG			IGMP_LKY_VLAN	IGMP_PRI_HIGH	IGMP_QUE_MIR	IGMP_QUE_FW		
Type	RW	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31	MDL_RPT_MIR	MLD Report/Done Message to Mirror Port 0: Disable 1: Frame copied to Mirror port
30:28	MLD_RPT_FW	MLD Report/Done Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped
27	MLD_MANG_FR	MLD Message as Management Frame 0: Disable 1: Regarded as management frame
26	MLD_PAE_FR	MLD Message as PAE Frame 0: Disable 1: Regarded as PAE frame
25	MLD_BPDU_FR	MLD Message as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	MLD_EG_TAG	MLD Message Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	MLD_LKY_VLAN	MLD Leaky VLAN Enable 0: Disable 1: Enable
20	MLD_PRI_HIGH	MLD Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
19	MLD_QUE_MIR	MLD Query Message to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	MLD_QUE_FW	MLD Query Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included

Bit(s)	Name	Description
15	IGMP_RPT_MIR	3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped IGMP Report/Done Message to Mirror Port 0: Disable 1: Frame copied to Mirror port
14:12	IGMP_RPT_FW	IGMP Report/Done Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame dropped
11	IGMP_MANG_FR	IGMP Message as Management Frame 0: Disable 1: Regarded as management frame
10	IGMP_PAE_FR	IGMP Message as PAE Frame 0: Disable 1: Regarded as PAE frame
9	IGMP_BPDU_FR	IGMP Message as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	IGMP_EG_TAG	IGMP Message Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	IGMP_LKY_VLAN	IGMP Leaky VLAN Enable 0: Disable 1: Enable
4	IGMP_PRI_HIGH	IGMP Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
3	IGMP_QUE_MIR	IGMP Query Message to Mirror Port 0: Disable 1: Frame copied to Mirror port
2:0	IGMP_QUE_FW	IGMP Query Message TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000020

APC

ARP and PPPoE Control

08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				PPP_MANG_FR	PPP_PAE_FR	PPP_BPDU_FR	PPP_EG_TAG			PPP_LKY_VLAN	PPP_PRI_HIGH	PPP_MIR	PPP_PORT_FW		
Type	RO				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				ARP_MANG_FR	ARP_PAE_FR	ARP_BPDU_FR	ARP_EG_TAG			ARP_LKY_VLAN	ARP_PRI_HIGH	ARP_MIR	ARP_PORT_FW		
Type	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	PPP_MANG_FR	PPPoE Discovery as Management Frame 0: Disable 1: Regarded as management frame
26	PPP_PAE_FR	PPPoE Discovery as PAE Frame 0: Disable 1: Regarded as PAE frame
25	PPP_BPDU_FR	PPPoE Discovery as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	PPP_EG_TAG	PPPoE Discovery Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	PPP_LKY_VLAN	PPPoE Discovery Leaky VLAN Enable 0: Disable 1: Enable
20	PPP_PRI_HIGH	PPPoE Discovery Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
19	PPP_MIR	PPPoE Discovery to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	PPP_PORT_FW	PPPoE Discovery TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	Reserved
11	ARP_MANG_FR	ARP/RARP Discovery as Management Frame 0: Disable 1: Regarded as management frame
10	ARP_PAE_FR	ARP/RARP Discovery as PAE Frame

Bit(s)	Name	Description
		0: Disable
9	ARP_BPDU_FR	1: Regarded as PAE frame ARP/RARP Discovery as BPDU Frame
		0: Non-BPDU Frame
8:6	ARP_EG_TAG	1: Regarded as BPDU frame ARP/RARP Discovery Egress VLAN Tag Attribution
		3'b000: System default (disable)
		3'b001: Consistent
		3'b010, 3'b011: Reserved
		3'b100: Untagged
		3'b101: Swap
		3'b110: Tagged
		3'b111: Stack
5	ARP_LKY_VLAN	ARP/RARP Discovery Leaky VLAN Enable
		0: Disable
		1: Enable
4	ARP_PRI_HIGH	ARP/RARP Discovery Force the Highest Priority
		0: System default
		1: Assigned to the highest priority queue.
3	ARP_MIR	ARP/RARP Discovery to Mirror Port
		0: Disable
		1: Frame copied to Mirror port
2:0	ARP_PORT_FW	ARP/RARP Discovery TO_CPU Forwarding
		3'b0xx: System default (disable)
		3'b100: System default and CPU port excluded
		3'b101: System default and CPU port included
		3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)
		3'b111: Frame Dropped

00000024				BPC	BPDU and PAE Control										0C100A10			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	REV0				PAE_MANG_FR	PAE_PAER_FR	PAE_BPDU_FR	PAE_EG_TAG			PAE_LKY_VLAN	PAE_PRI_HIGH	PAE_MIR	PAE_PORT_FW				
Type	RO				RW	RW	RW	RW			RW	RW	RW	RW				
Reset	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	REV1				BPDU_MANG_FR	BPDU_PAER_FR	BPDU_BPDU_FR	BPDU_EG_TAG			BPDU_LKY_VLAN	BPDU_PRI_HIGH	BPDU_MIR	BPDU_PORT_FW				
Type	RW				RW	RW	RW	RW			RW	RW	RW	RW				
Reset	0	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0		

Bit(s)	Name	Description
31:28	REV0	Reserved
27	PAE_MANG_FR	PAE as Management Frame
		0: Disable
		1: Regarded as management frame
26	PAE_PAER_FR	PAE as PAE Frame

Bit(s)	Name	Description
		0: Disable
25	PAE_BPDU_FR	1: Regarded as PAE frame PAE as BPDU Frame
		0: Non-BPDU Frame
24:22	PAE_EG_TAG	1: Regarded as BPDU frame PAE Egress VLAN Tag Attribution
		3'b000: System default (disable)
		3'b001: Consistent
		3'b010, 3'b011: Reserved
		3'b100: Untagged
		3'b101: Swap
		3'b110: Tagged
		3'b111: Stack
21	PAE_LKY_VLAN	PAE Leaky VLAN Enable
		0: Disable
		1: Enable
20	PAE_PRI_HIGH	PAE Force the Highest Priority
		0: System default
		1: Assigned to the highest priority queue.
19	PAE_MIR	PAE to Mirror Port
		0: Disable
		1: Frame copied to Mirror port
18:16	PAE_PORT_FW	PAE TO_CPU Forwarding
		3'b0xx: System default (disable)
		3'b100: System default and CPU port excluded
		3'b101: System default and CPU port included
		3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)
		3'b111: Frame Dropped
15:12	REV1	Reserved
11	BPDU_MANG_FR	BPDU as Management Frame
		0: Disable
		1: Regarded as management frame
10	BPDU_PAE_FR	BPDU as PAE Frame
		0: Disable
		1: Regarded as PAE frame
9	BPDU_BPDU_FR	BPDU as BPDU Frame
		0: Non-BPDU Frame
		1: Regarded as BPDU frame
8:6	BPDU_EG_TAG	BPDU Egress VLAN Tag Attribution
		3'b000: System default (disable)
		3'b001: Consistent
		3'b010, 3'b011: Reserved
		3'b100: Untagged
		3'b101: Swap
		3'b110: Tagged
		3'b111: Stack
5	BPDU_LKY_VLAN	BPDU Leaky VLAN Enable
		0: Disable
		1: Enable
4	BPDU_PRI_HIGH	BPDU Force the Highest Priority
		0: System default

Bit(s)	Name	Description
3	BPDU_MIR	1: Assigned to the highest priority queue. BPDU to Mirror Port 0: Disable
2:0	BPDU_PORT_FW	1: Frame copied to Mirror port BPDU TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000028 RGAC1 REV_01 and REV_02 Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				R02_MANG_FR	R02_PAE_FR	R02_BPDU_FR	R02_EG_TAG			R02_LKY_VLAN	R02_PRI_HIGH	R02_MIR	R02_PORT_FW		
Type	RO				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R01_MANG_FR	R01_PAE_FR	R01_BPDU_FR	R01_EG_TAG			R01_LKY_VLAN	R01_PRI_HIGH	R01_MIR	R01_PORT_FW		
Type	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	R02_MANG_FR	REV_02 as Management Frame 0: Disable 1: Regarded as management frame
26	R02_PAE_FR	REV_02 as PAE Frame 0: Disable 1: Regarded as PAE frame
25	R02_BPDU_FR	REV_02 as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	R02_EG_TAG	REV_02 Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	R02_LKY_VLAN	REV_02 Leaky VLAN Enable 0: Disable 1: Enable
20	R02_PRI_HIGH	REV_02 Force the Highest Priority 0: System default

Bit(s)	Name	Description
19	R02_MIR	1: Assigned to the highest priority queue. REV_02 to Mirror Port 0: Disable
18:16	R02_PORT_FW	1: Frame copied to Mirror port REV_02 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	Reserved
11	R01_MANG_FR	REV_01 as Management Frame 0: Disable 1: Regarded as management frame
10	R01_PAE_FR	REV_01 as PAE Frame 0: Disable 1: Regarded as PAE frame
9	R01_BPDU_FR	REV_01 as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R01_EG_TAG	REV_01 Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R01_LKY_VLAN	REV_01 Leaky VLAN Enable 0: Disable 1: Enable
4	R01_PRI_HIGH	REV_01 Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
3	R01_MIR	REV_01 to Mirror Port 0: Disable 1: Frame copied to Mirror port
2:0	R01_PORT_FW	REV_01 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

0000002C	RGAC2				REV_03 and REV_0E Control								08100810			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	REV0				R0E_MANG_FR	R0E_PAE_FR	R0E_BPDU_FR	R0E_EG_TAG			R0E_LKY_VLAN	R0E_PRI_HIGH	R0E_MIR	R0E_PORT_FW		
Type	RO				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R03_MANG_FR	R03_PAE_FR	R03_BPDU_FR	R03_EG_TAG			R03_LKY_VLAN	R03_PRI_HIGH	R03_MIR	R03_PORT_FW		
Type	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	R0E_MANG_FR	REV_0E as Management Frame 0: Disable 1: Regarded as management frame
26	R0E_PAE_FR	REV_0E as PAE Frame 0: Disable 1: Regarded as PAE frame
25	R0E_BPDU_FR	REV_0E as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	R0E_EG_TAG	REV_0E Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	R0E_LKY_VLAN	REV_0E Leaky VLAN Enable 0: Disable 1: Enable
20	R0E_PRI_HIGH	REV_0E Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
19	R0E_MIR	REV_0E to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	R0E_PORT_FW	REV_0E TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	Reserved
11	R03_MANG_FR	REV_03 as Management Frame 0: Disable 1: Regarded as management frame
10	R03_PAE_FR	REV_03 as PAE Frame 0: Disable

Bit(s)	Name	Description
9	R03_BPDU_FR	1: Regarded as PAE frame REV_03 as BPDU Frame 0: Non-BPDU Frame
8:6	R03_EG_TAG	1: Regarded as BPDU frame REV_03 Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R03_LKY_VLAN	REV_03 Leaky VLAN Enable 0: Disable 1: Enable
4	R03_PRI_HIGH	REV_03 Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
3	R03_MIR	REV_03 to Mirror Port 0: Disable 1: Frame copied to Mirror port
2:0	R03_PORT_FW	REV_03 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000030 **RGAC3** **REV_10 and REV_20 Control** 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				R20_MANG_FR	R20_PAE_FR	R20_BPDU_FR	R20_EG_TAG			R20_LKY_VLAN	R20_PRI_HIGH	R20_MIR	R20_PORT_FW		
Type	RO				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R10_MANG_FR	R10_PAE_FR	R10_BPDU_FR	R10_EG_TAG			R10_LKY_VLAN	R10_PRI_HIGH	R10_MIR	R10_PORT_FW		
Type	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	R20_MANG_FR	REV_20 as Management Frame 0: Disable 1: Regarded as management frame
26	R20_PAE_FR	REV_20 as PAE Frame 0: Disable

Bit(s)	Name	Description
25	R20_BPDU_FR	1: Regarded as PAE frame REV_20 as BPDU Frame 0: Non-BPDU Frame
24:22	R20_EG_TAG	1: Regarded as BPDU frame REV_20 Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	R20_LKY_VLAN	REV_20 Leaky VLAN Enable 0: Disable 1: Enable
20	R20_PRI_HIGH	REV_20 Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
19	R20_MIR	REV_20 to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	R20_PORT_FW	REV_20 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	Reserved
11	R10_MANG_FR	REV_10 as Management Frame 0: Disable 1: Regarded as management frame
10	R10_PAE_FR	REV_10 as PAE Frame 0: Disable 1: Regarded as PAE frame
9	R10_BPDU_FR	REV_10 as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R10_EG_TAG	REV_10 Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R10_LKY_VLAN	REV_10 Leaky VLAN Enable 0: Disable 1: Enable
4	R10_PRI_HIGH	REV_10 Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.

Bit(s)	Name	Description
3	R10_MIR	REV_10 to Mirror Port 0: Disable 1: Frame copied to Mirror port
2:0	R10_PORT_FW	REV_10 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000034 RGAC4 REV_21 and REV_UN Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				RUN_MANG_FR	RUN_PAE_FR	RUN_BPDU_FR	RUN_EG_TAG			RUN_LKY_VLAN	RUN_PRI_HIGH	RUN_MIR	RUN_PORT_FW		
Type	RO				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				R21_MANG_FR	R21_PAE_FR	R21_BPDU_FR	R21_EG_TAG			R21_LKY_VLAN	R21_PRI_HIGH	R21_MIR	R21_PORT_FW		
Type	RW				RW	RW	RW	RW			RW	RW	RW	RW		
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	RUN_MANG_FR	REV_20 as Management Frame 0: Disable 1: Regarded as management frame
26	RUN_PAE_FR	REV_20 as PAE Frame 0: Disable 1: Regarded as PAE frame
25	RUN_BPDU_FR	REV_20 as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	RUN_EG_TAG	REV_20 Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	RUN_LKY_VLAN	REV_20 Leaky VLAN Enable 0: Disable 1: Enable
20	RUN_PRI_HIGH	REV_20 Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.

Bit(s)	Name	Description
19	RUN_MIR	REV_20 to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	RUN_PORT_FW	REV_20 TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	Reserved
11	R21_MANG_FR	REV_UN as Management Frame 0: Disable 1: Regarded as management frame
10	R21_PAE_FR	REV_UN as PAE Frame 0: Disable 1: Regarded as PAE frame
9	R21_BPDU_FR	REV_UN as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	R21_EG_TAG	REV_UN Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	R21_LKY_VLAN	REV_UN Leaky VLAN Enable 0: Disable 1: Enable
4	R21_PRI_HIGH	REV_UN Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
3	R21_MIR	REV_UN to Mirror Port 0: Disable 1: Frame copied to Mirror port
2:0	R21_PORT_FW	REV_UN TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped

00000038	PMC										Protocol Match Control						00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	REV0		TYPE3_EN	TYPE3_VLD	TYPE3_ENCAP				REV1		TYPE2_EN	TYPE2_VLD	TYPE2_ENCAP							

Type	RW		RW	RW	RW				RW		RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2		TYPE1_EN	TYPE1_VLD	TYPE1_ENCAP				REV3							
Type	RW		RW	RW	RW				RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	Reserved
29	TYPE3_EN	TYPE 3 Match Enable
28	TYPE3_VLD	TYPE 3 Value Valid
27:24	TYPE3_ENCAP	Encapsulated Frame Type Value
23:22	REV1	Reserved
21	TYPE2_EN	TYPE 2 Match Enable
20	TYPE2_VLD	TYPE 2 Value Valid
19:16	TYPE2_ENCAP	Encapsulated Frame Type Value
15:14	REV2	Reserved
13	TYPE1_EN	TYPE 1 Match Enable
12	TYPE1_VLD	TYPE 1 Value Valid
		0: TYPE 1 Value in register PBG.TYPE1 is "don't care", i.e. it has no effect.
		1: TYPE 1 Value in register PBG.TYPE1 is valid.
11:8	TYPE1_ENCAP	Encapsulated Frame Type Value
		Bit0: Ethernet II
		Bit1: RFC_1042
		Bit2: IPX Raw 802.3
		Bit3: 802.2/802.3 Length Encapsulated
7:0	REV3	Reserved

0000003C PBG1 Protocol Based Group ID-1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TYPE1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TYPE1	TYPE 1 Value
		Ethernet II: Matched with EtherType
		RFC_1042: Matched with SNAP Type
		IPX Raw 802.3: "Don't care"
		802.2/802.3 Length Encapsulate: Matched with DSAP[15:8] and SSAP[7:0]
15:0	REV0	Reserved

00000040 PBG2 Protocol Based Group ID-2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TYPE3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TYPE2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	TYPE3	TYPE 3 Value
15:0	TYPE2	TYPE 2 Value

00000058 PIM1 DSCP Priority Ingress Mapping I 09000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_09			PRI_DSCP_08			PRI_DSCP_07			PRI_DSCP_06			PRI_DSCP_05	
Type	RO		RW			RW			RW			RW			RW	
Reset	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DS CP_05		PRI_DSCP_04			PRI_DSCP_03			PRI_DSCP_02			PRI_DSCP_01			PRI_DSCP_00	
Type	RW		RW			RW			RW			RW			RW	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:30	REV0	Reserved
29:27	PRI_DSCP_09	User Priority for Differentiated Services Code Point (DSCP) 0b001_001
26:24	PRI_DSCP_08	User Priority for DSCP 0b001_000
23:21	PRI_DSCP_07	User Priority for DSCP 0b000_111
20:18	PRI_DSCP_06	User Priority for DSCP 0b000_110
17:15	PRI_DSCP_05	User Priority for DSCP 0b000_101
14:12	PRI_DSCP_04	User Priority for DSCP 0b000_100
11:9	PRI_DSCP_03	User Priority for DSCP 0b000_011
8:6	PRI_DSCP_02	User Priority for DSCP 0b000_010
5:3	PRI_DSCP_01	User Priority for DSCP 0b000_001
2:0	PRI_DSCP_00	User Priority for DSCP 0b000_000

0000005C PIM2 DSCP Priority Ingress Mapping II 12489249

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_19			PRI_DSCP_18			PRI_DSCP_17			PRI_DSCP_16			PRI_DSCP_15	
Type	RO		RW			RW			RW			RW			RW	
Reset	0	0	0	1	0	0	1	0	0	1	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DS CP_15		PRI_DSCP_14			PRI_DSCP_13			PRI_DSCP_12			PRI_DSCP_11			PRI_DSCP_10	
Type	RW		RW			RW			RW			RW			RW	
Reset	1	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1

Bit(s)	Name	Description
31:30	REVO	Reserved
29:27	PRI_DSCP_19	User Priority for DSCP 0b010_011
26:24	PRI_DSCP_18	User Priority for DSCP 0b010_010
23:21	PRI_DSCP_17	User Priority for DSCP 0b010_001
20:18	PRI_DSCP_16	User Priority for DSCP 0b010_000
17:15	PRI_DSCP_15	User Priority for DSCP 0b001_111
14:12	PRI_DSCP_14	User Priority for DSCP 0b001_110
11:9	PRI_DSCP_13	User Priority for DSCP 0b001_101
8:6	PRI_DSCP_12	User Priority for DSCP 0b001_100
5:3	PRI_DSCP_11	User Priority for DSCP 0b001_011
2:0	PRI_DSCP_10	User Priority for DSCP 0b001_010

00000060 **PIM3** DSCP Priority Ingress Mapping III 1B6DB492

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO		PRI_DSCP_29			PRI_DSCP_28			PRI_DSCP_27			PRI_DSCP_26			PRI_DSCP_25	
Type	RO		RW			RW			RW			RW			RW	
Reset	0	0	0	1	1	0	1	1	0	1	1	0	1	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DS CP_25	PRI_DSCP_24			PRI_DSCP_23			PRI_DSCP_22			PRI_DSCP_21			PRI_DSCP_20		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	0	1	1	0	1	0	0	1	0	0	1	0	0	1	0

Bit(s)	Name	Description
31:30	REVO	Reserved
29:27	PRI_DSCP_29	User Priority for DSCP 0b011_101
26:24	PRI_DSCP_28	User Priority for DSCP 0b011_100
23:21	PRI_DSCP_27	User Priority for DSCP 0b011_011
20:18	PRI_DSCP_26	User Priority for DSCP 0b011_010
17:15	PRI_DSCP_25	User Priority for DSCP 0b011_001
14:12	PRI_DSCP_24	User Priority for DSCP 0b011_000
11:9	PRI_DSCP_23	User Priority for DSCP 0b010_111
8:6	PRI_DSCP_22	User Priority for DSCP 0b010_110
5:3	PRI_DSCP_21	User Priority for DSCP 0b010_101
2:0	PRI_DSCP_20	User Priority for DSCP 0b010_100

00000064 **PIM4** DSCP Priority Ingress Mapping IV 2492491B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO		PRI_DSCP_39			PRI_DSCP_38			PRI_DSCP_37			PRI_DSCP_36			PRI_DSCP_35	
Type	RO		RW			RW			RW			RW			RW	
Reset	0	0	1	0	0	1	0	0	1	0	0	1	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DS CP_35	PRI_DSCP_34			PRI_DSCP_33			PRI_DSCP_32			PRI_DSCP_31			PRI_DSCP_30		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	1	0	0	1	0	0	1	0	0	0	1	1	0	1	1

Bit(s)	Name	Description
31:30	REVO	Reserved

Bit(s)	Name	Description
29:27	PRI_DSCP_39	User Priority for DSCP 0b100_111
26:24	PRI_DSCP_38	User Priority for DSCP 0b100_110
23:21	PRI_DSCP_37	User Priority for DSCP 0b100_101
20:18	PRI_DSCP_36	User Priority for DSCP 0b100_100
17:15	PRI_DSCP_35	User Priority for DSCP 0b100_011
14:12	PRI_DSCP_34	User Priority for DSCP 0b100_010
11:9	PRI_DSCP_33	User Priority for DSCP 0b100_001
8:6	PRI_DSCP_32	User Priority for DSCP 0b100_000
5:3	PRI_DSCP_31	User Priority for DSCP 0b011_111
2:0	PRI_DSCP_30	User Priority for DSCP 0b011_110

00000068 PIM5 DSCP Priority Ingress Mapping V 36B6DB6D

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_49			PRI_DSCP_48			PRI_DSCP_47			PRI_DSCP_46			PRI_DSCP_45	
Type	RO		RW			RW			RW			RW			RW	
Reset	0	0	1	1	0	1	1	0	1	0	1	1	0	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DS CP_45	PRI_DSCP_44			PRI_DSCP_43			PRI_DSCP_42			PRI_DSCP_41			PRI_DSCP_40		
Type	RW	RW			RW			RW			RW			RW		
Reset	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0	1

Bit(s)	Name	Description
31:30	REV0	Reserved
29:27	PRI_DSCP_49	User Priority for DSCP 0b110_001
26:24	PRI_DSCP_48	User Priority for DSCP 0b110_000
23:21	PRI_DSCP_47	User Priority for DSCP 0b101_111
20:18	PRI_DSCP_46	User Priority for DSCP 0b101_110
17:15	PRI_DSCP_45	User Priority for DSCP 0b101_101
14:12	PRI_DSCP_44	User Priority for DSCP 0b101_100
11:9	PRI_DSCP_43	User Priority for DSCP 0b101_011
8:6	PRI_DSCP_42	User Priority for DSCP 0b101_010
5:3	PRI_DSCP_41	User Priority for DSCP 0b101_001
2:0	PRI_DSCP_40	User Priority for DSCP 0b101_000

0000006C PIM6 DSCP Priority Ingress Mapping VI 3FFF6DB6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0		PRI_DSCP_59			PRI_DSCP_58			PRI_DSCP_57			PRI_DSCP_56			PRI_DSCP_55	
Type	RO		RW			RW			RW			RW			RW	
Reset	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PRI_DS CP_55	PRI_DSCP_54			PRI_DSCP_53			PRI_DSCP_52			PRI_DSCP_51			PRI_DSCP_50		
Type	RW	RW			RW			RW			RW			RW		
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	1	1	0

Bit(s)	Name	Description
31:30	REV0	Reserved
29:27	PRI_DSCP_59	User Priority for DSCP 0b111_011

Bit(s)	Name	Description
26:24	PRI_DSCP_58	User Priority for DSCP 0b111_010
23:21	PRI_DSCP_57	User Priority for DSCP 0b111_001
20:18	PRI_DSCP_56	User Priority for DSCP 0b111_000
17:15	PRI_DSCP_55	User Priority for DSCP 0b110_111
14:12	PRI_DSCP_54	User Priority for DSCP 0b110_110
11:9	PRI_DSCP_53	User Priority for DSCP 0b110_101
8:6	PRI_DSCP_52	User Priority for DSCP 0b110_100
5:3	PRI_DSCP_51	User Priority for DSCP 0b110_011
2:0	PRI_DSCP_50	User Priority for DSCP 0b110_010

00000070 **PIM7** DSCP Priority Ingress Mapping VII 00000FFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO				PRI_DSCP_63			PRI_DSCP_62			PRI_DSCP_61			PRI_DSCP_60		
Type	RO				RW			RW			RW			RW		
Reset	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:12	REVO	Reserved
11:9	PRI_DSCP_63	User Priority for DSCP 0b111_111
8:6	PRI_DSCP_62	User Priority for DSCP 0b111_110
5:3	PRI_DSCP_61	User Priority for DSCP 0b111_101
2:0	PRI_DSCP_60	User Priority for DSCP 0b111_100

00000074 **ATA1** Address Table Access I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	MAC Address[47:40] / Destination IP(DIP) Address [31:24]
23:16	BYTE_1	MAC Address[39:32] / Destination IP(DIP) Address [23:16]
15:8	BYTE_2	MAC Address[31:24] / Destination IP(DIP) Address [15:8]
7:0	BYTE_3	MAC Address[23:16] / Destination IP(DIP) Address [7:0]

00000078 **ATA2** Address Table Access II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							

Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	MAC Address[15:8] / Source IP(SIP) Address [31:24]
23:16	BYTE_1	MAC Address[7:0] / Source IP(SIP) Address [23:16]
15:8	BYTE_2	SIP Address [15: 8] or bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table.
7:0	BYTE_3	SIP Address[7:0] or CVID[7:0]

0000007C ATWD Address Table Write Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	Table Write Data

00000080 ATC Address Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO			COL_A CC	ADDR											
Type	RO			RO	RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BUSY	SRCH_E ND	SRCH_ HIT	ADDR_I NVLD	AC_MAT				REV1		AC_SAT		AC_CA E	AC_CMD		
Type	W1S	RO	RO	RO	RW				RW		RW		RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:29	REVO	Reserved
28	COL_ACC	Access Target is Collision Pool Read/Write command is applied to collision pool

Bit(s)	Name	Description
		0: Address Table 1: Collision Pool
27:16	ADDR	Address Table Access Index The actual address table access index which is calculated from a 48-bit MAC address, a 32-bit DIP, and a SIP address. (for debugging purposes)
15	BUSY	Address Table Is Busy SW can set this bit to 1 only if this bit is reset. After ATWD registers are written and this bit is set, this chip will perform the corresponding function according to AC_CMD, AC_SAT, and AC_MAT included in this register.
14	SRCH_END	Linear Search End The linear search has reached the index end of the address table. For Search Command Only (AC_CMD=3'b100 or 3'b101)
13	SRCH_HIT	Linear Search Hit The linear search has find the target based on AC_MAT and return the data on TSRA1,2 and ATRD. If this register is not TRUE(1) after search command completed, that means nothing found and data on TSRA1,2 and ATRD are invalid. For Search Command Only (AC_CMD=3'b100 or 3'b101)
12	ADDR_INVLD	Address Entry is not Valid Read Operations: The specified entry is not valid for read or removal access. Read Data returned on TSRA1, TSRA2 and ATRD are invalid. Write Operations: The specified entry cannot be modified or added for write access. For Single Entry Read/Write Only (AC_CMD=3'b000 or 3'b001).
11:8	AC_MAT	Address Table Multiple Access Target Whenever MATC register is written and bit.15 is set, this chip will perform the corresponding function on the Address table based on AC_CMD bits. 4'b0000: All MAC address entries 4'b0001: All DIP/GA address entries 4'b0010: All SIP address entries 4'b0011: All valid address entry 4'b0100: All non-static MAC address entries. 4'b0101: All non-static DIP address entries. 4'b0110: All static MAC address entries 4'b0111: All static DIP address entries 4'b1000: All relative SIP address entries based on the specific DIP from ATA2 register. 4'b1001: All relative SIP address entries based on the specific SIP from ATA2 register. 4'b1010: All MAC Address entries with the customer VID specified in ATA2.CVID[11:0] 4'b1010: All MAC address entries with the Filter ID specified in ATA2.FID[2:0] 4'b1100: All MAC Address entries with the source ports specified in ATA1.PORT[7:0] 4'b1101 to 4'b1111: Reserved
7:6	REV1	Reserved
5:4	AC_SAT	Address Table Single Access Target Whenever MATC register is written and bit.31 is set, this chip will perform the corresponding function on the Address table based on FUNC bits. 2'b00: Specified MAC address entry 2'b01: Specified DIP address entry 2'b10: Specified SIP address entry

Bit(s)	Name	Description
3	AC_CAE	2'b11: Specified address entry(read only) Collision Pool Access Enable For Read and Write command(single entry), read/write collision pool while address table hash collision. For Clean and Search command, access target is collision pool (not to access address table) If Collision Pool is disabled, this register is invalid. 0: Disable 1: Enable
2:0	AC_CMD	Address Table Access Command 3'b000: Read command (single entry) 3'b001: Write command (single entry) NOTE: Supports modify, add, and remove 3'b010: Clean command (multiple entries) 3'b011: Reserved 3'b100: Start Search command (reset to 1st entry) 3'b101: Next Search command (next entry) 3'b110 to 3'b111: Reserved

00000084		TSRA1		Table Search Read Address I												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	BYTE_0								BYTE_1								
Type	RO								RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	BYTE_2								BYTE_3								
Type	RO								RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:24	BYTE_0	MAC Address[47:40] / Destination IP(DIP) Address [31:24] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished
23:16	BYTE_1	MAC Address[39:32] / Destination IP(DIP) Address [23:16] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished
15:8	BYTE_2	MAC Address[31:24] / Destination IP(DIP) Address [15:8] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished
7:0	BYTE_3	MAC Address[23:16] / Destination IP(DIP) Address [7:0] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished

00000088 TSRA2 Table Search Read Address II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BYTE_0								BYTE_1							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BYTE_2								BYTE_3							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	BYTE_0	MAC Address[15:8] / Source IP(SIP) Address [31:24] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished
23:16	BYTE_1	MAC Address[7:0] / Source IP(SIP) Address [23:16] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished
15:8	BYTE_2	SIP Address [15: 8] or bit[15]: IVL bit[14:12]: Filter ID[2:0] bit[11:8]: CVID[11: 8] NOTE: When IVL is reset, MAC[47:0] and FID[2:0] will be used to read/write the address table. When IVL is set, MAC[47:0] and CVID[11:0] will be used to read/write the address table. The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished
7:0	BYTE_3	SIP Address[7:0] or CVID[7:0] The data on this register is invalid if the following is true: Read/Write Operation: ADDR_INVLD=1 after the operation finished Search Operation: SRCH_HIT=0 after the operation finished

0000008C ATRD Address Table Read Data 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RDATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDATA															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RDATA	Table Read Data

Bit(s)	Name	Description

The data on this register is invalid if the following is true:
Read/Write Operation: ADDR_INVLD=1 after the operation finished
Search Operation: SRCH_HIT=0 after the operation finished

00000090 VTCTR VLAN Table Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	BUSY	REV0														IDX_IN VLD
Type	W1S	RO														RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FUNC				VID											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	BUSY	VLAN Table Is Busy SW can set this bit to 1 only if this bit is reset. After the VTCTR register is written and this bit is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits.
30:17	REV0	Reserved
16	IDX_INVLD	Entry is not Valid This index for the access control is out of the valid index.
15:12	FUNC	Access Control Function Whenever VTCTR register is written and bit.31 is set, this chip will perform the corresponding function on the VLAN table based on FUNC bits. 4'b0000: Read the specified VID Entry from VAWD# register based on VID bits 4'b0001: Write the specified VID Entry though VAWD# register based on VID bits. 4'b0010: Make the specified VID entry invalid based on VID bits. 4'b0011: Make the specified VID entry valid based on VID bits. 4'b0100: Read the specified ACL Table entry. 4'b0101: Write the specified ACL Table entry. 4'b0110: Read the specified trTCM Meter Table. 4'b0111: Write the specified trTCM Meter Table. 4'b1000: Read the specified ACL Mask entry. 4'b1001: Write the specified ACL Mask entry. 4'b1010: Read the specified ACL Rule Control entry. 4'b1011: Write the specified ACL Rule Control entry. 4'b1100: Read the specified ACL Rate Control entry. 4'b1101: Write the specified ACL Rate Control entry. 4'b1110: Reserved 4'b1111: Reserved
11:0	VID	1. VLAN ID Number: 0x0 to 0x1F (16) 2. ACL table index: 0x0 to 0xFF (256) 3. ACL mask control: 0x0 to 0x7F (128)

00000094 VAWD1 VLAN and ACL Write Data I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	VLAN Table Write Data I

00000098 VAWD2 VLAN and ACL Write Data II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	VLAN Table Write Data II

0000009C TRTCM Two Rate Three Color Mark 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TRTCM_EN	REVO														
Type	RW	RW														
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	TRTCM_EN	Two Rate Three Color Marker (trTCM) Enable When this bit is enabled, the meter table will be updated based on Peak Information Rate (PIR) and Committed Information Rate (CIR). The color marker will also be enabled when ACL is hit. 0: Disable 1: Enable
30:0	REVO	Reserved

000000A0 AAC Address Age Control 00095001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												AGE_DIS	AGE_CNT			
Type												RW	RW			
Reset												0	1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_CNT				AGE_UNIT											
Type	RW				RW											
Reset	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
20	AGE_DIS	Address Table Aging Disable Disable or pause MAC address aging.
19:12	AGE_CNT	Address Table Age Count This age count is recorded in the age timer field of the MAC address table when a new source address is received and the table entry is ready to refresh the timer. The applied age timer is equal to (AGE_CNT+1) *(AGE_UNIT+1) seconds.
11:0	AGE_UNIT	Address Table Age Unit The applied aging unit is equal to (AGE_UNIT+1) seconds.

000000A4 DHCP DHCP Control 08100810

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				DHCPv6_MANG_FR	DHCPv6_PAE_FR	DHCPv6_BPDU_FR	DHCPv6_EG_TAG				DHCPv6_LKY_VLAN	DHCPv6_PRI_HIGH	DHCPv6_MIR	DHCPv6_PORT_FW	
Type	RO				RW	RW	RW	RW				RW	RW	RW	RW	
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1				DHCPv4_MANG_FR	DHCPv4_PAE_FR	DHCPv4_BPDU_FR	DHCPv4_EG_TAG				DHCPv4_LKY_VLAN	DHCPv4_PRI_HIGH	DHCPv4_MIR	DHCPv4_PORT_FW	
Type	RW				RW	RW	RW	RW				RW	RW	RW	RW	
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	DHCPv6_MANG_FR	DHCPv6 Discovery/Request as Management Frame 0: Disable 1: Regarded as management frame
26	DHCPv6_PAE_FR	DHCPv6 Discovery/Request as PAE Frame 0: Disable 1: Regarded as PAE frame
25	DHCPv6_BPDU_FR	DHCPv6 Discovery/Request as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	DHCPv6_EG_TAG	DHCPv6 Discovery/Request Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved

Bit(s)	Name	Description
		3'b100: Untagged
		3'b101: Swap
		3'b110: Tagged
		3'b111: Stack
21	DHCPv6_LKY_VLAN	DHCPv6 Discovery/Request Leaky VLAN Enable 0: Disable 1: Enable
20	DHCPv6_PRI_HIGH	DHCPv6 Discovery/Request Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
19	DHCPv6_MIR	DHCPv6 Discovery/Request to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	DHCPv6_PORT_FW	DHCPv6 Discovery/Request TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.) 3'b111: Frame Dropped
15:12	REV1	Reserved
11	DHCPv4_MANG_FR	DHCPv4 Discovery/Request as Management Frame 0: Disable 1: Regarded as management frame
10	DHCPv4_PAE_FR	DHCPv4 Discovery/Request as PAE Frame 0: Disable 1: Regarded as PAE frame
9	DHCPv4_BPDU_FR	DHCPv4 Discovery/Request as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
8:6	DHCPv4_EG_TAG	DHCPv4 Discovery/Request Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
5	DHCPv4_LKY_VLAN	DHCPv4 Discovery/Request Leaky VLAN Enable 0: Disable 1: Enable
4	DHCPv4_PRI_HIGH	DHCPv4 Discovery/Request Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
3	DHCPv4_MIR	DHCPv4 Discovery/Request to Mirror Port 0: Disable 1: Frame copied to Mirror port
2:0	DHCPv4_PORT_FW	DHCPv4 Discovery/Request TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included

Bit(s)	Name	Description
		3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)
		3'b111: Frame Dropped

000000A8 LCP PPPoE LCP Control 08100000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0				PPP_LCP_P_MANG_FR	PPP_LCP_P_PAE_FR	PPP_LCP_P_BPDU_FR	PPP_LCP_EG_TAG				PPP_LCP_P_LKY_VLAN	PPP_LCP_P_PRI_HIGH	PPP_LCP_P_MIR	PPP_LCP_PORT_FW	
Type	RW				RW	RW	RW	RW				RW	RW	RW	RW	
Reset	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:28	REV0	Reserved
27	PPP_LCP_MANG_FR	PPPoE Session LCP as Management Frame 0: Disable 1: Regarded as management frame
26	PPP_LCP_PAE_FR	PPPoE Session LCP as PAE Frame 0: Disable 1: Regarded as PAE frame
25	PPP_LCP_BPDU_FR	PPPoE Session LCP as BPDU Frame 0: Non-BPDU Frame 1: Regarded as BPDU frame
24:22	PPP_LCP_EG_TAG	PPPoE Session LCP Egress VLAN Tag Attribution 3'b000: System default (disable) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
21	PPP_LCP_LKY_VLAN	PPPoE Session LCP Leaky VLAN Enable 0: Disable 1: Enable
20	PPP_LCP_PRI_HIGH	PPPoE Session LCP Force the Highest Priority 0: System default 1: Assigned to the highest priority queue.
19	PPP_LCP_MIR	PPPoE Session LCP to Mirror Port 0: Disable 1: Frame copied to Mirror port
18:16	PPP_LCP_PORT_FW	PPPoE Session LCP TO_CPU Forwarding 3'b0xx: System default (disable) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included

Bit(s)	Name	Description
		3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, then the system default and CPU port are excluded.)
		3'b111: Frame Dropped
15:0	REV1	Reserved

000000AC	MHS		MAC Table Hash Seed												FFFFFFFF		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	CRC_SEED																
Type	RW																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	CRC_SEED																
Type	RW																
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	

Bit(s)	Name	Description
31:0	CRC_SEED	MAC Table Hash CRC16/CRC32 Seed CRC32 : bit [31:0] CRC16 : bit [15:0]

000000B0	CPGC		Collision Pool Global Control										00000017			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													COL_B USY	COL_RS T_N	COL_CL K_EN	COL_E N
Type													RO	RW	RW	RW
Reset													0	1	1	1

Bit(s)	Name	Description
3	COL_BUSY	Collision Pool is Busy 0: IDLE 1: BUSY
2	COL_RST_N	Collision Pool Soft Reset Active Low. Before reset collision pool, it must be disabled and is not busy 0: Reset activated 1: Not activated
1	COL_CLK_EN	Collision Pool Clock Enable Before enable/disable collision pool clock, collision pool must be disabled and is not busy 0: Disable 1: Enable
0	COL_EN	Collision Pool Enable

Bit(s)	Name	Description
		Do NOT enable collision pool while collision pool soft reset activated
		0: Disable
		1: Enable

000000B4 CPMONC Collision Pool Monitor Control												00070020				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												COL_F ULL_CN T_CLR	COL_C NT_CLR	COL_CNT_CTRL		
Type												W1S	W1S	RW		
Reset												0	0	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		COL_USED_CNT										COL_E MPTY	COL_F ULL	COL_F ULL_CN T_EN	COL_C NT_EN	COL_MON_SEL
Type		RO										RO	RO	RW	RW	RW
Reset		0	0	0	0	0	0	0			1	0	0	0	0	0

Bit(s)	Name	Description
20	COL_FULL_CNT_CLR	Full and Collision Counter Reset Return to 0 automatically after reset done 0: Reset Released 1: Reset Active
19	COL_CNT_CLR	Address Table Collision Counter Reset Return to 0 automatically after reset done 0: Reset Released 1: Reset Active
18:16	COL_CNT_CTRL	Collision Type Bit Map for Collision Counters The type of collision for counters. To enable the specific type, set corresponding bits to 1. BIT 0: DIP Table Collision BIT 1: SA Learning Collision BIT 2: CSR Path Write Access Collision
14:8	COL_USED_CNT	Collision Pool used entry counter
5	COL_EMPTY	Collision Pool is empty 0: Not empty 1: Empty
4	COL_FULL	Collision Pool is full 0: Not full 1: Full
3	COL_FULL_CNT_EN	Full and Collision Counter Enable 0: Disable 1: Enable
2	COL_CNT_EN	Address Table Collision Counter Enable 0: Disable 1: Enable
1:0	COL_MON_SEL	Collision Pool Entry Status Monitor Selection Select which type of entries are shown in Entry Status Monitor CPMOND1 and CPMOND2 2'b00: Empty entry

Bit(s)	Name	Description
		2'b01: Dynamic entry
		2'b10: Reserved entry
		2'b11: Static entry

000000B8 CPMOND1 Collision Pool Entry Status Monitor 1 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENTRY															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENTRY															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	ENTRY	Collision Pool Entry Status Monitor Bit map of entry 31~0 0: Not hit selected status 1: Hit selected status

000000BC CPMOND2 Collision Pool Entry Status Monitor 2 FFFFFFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ENTRY															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ENTRY															
Type	RO															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:0	ENTRY	Collision Pool Entry Status Monitor Bit map of entry 63~32 0: Not hit selected status 1: Hit selected status

000000C0 CPSTSC Collision Pool Status Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	COL_FULL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	COL_FULL_CNT	Full and Collision Counter Address Table Collision when Collision Pool is Full Counter disabled automatically when Collision Pool disabled
15:0	COL_CNT	Address Table Collision Counter

000000C4 AISR_EXT1 ACL Extension Interrupt Status I 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_ISR_EXT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACL_ISR_EXT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ACL_ISR_EXT	ACL Interrupt Status for entry 32~63

000000C8 AISR_EXT2 ACL Extension Interrupt Status II 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_ISR_EXT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACL_ISR_EXT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ACL_ISR_EXT	ACL Interrupt Status for entry 64~95

000000CC AISR_EXT3 ACL Extension Interrupt Status III 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_ISR_EXT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ACL_ISR_EXT															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	ACL_ISR_EXT	ACL Interrupt Status for entry 96~127

000000D0	<u>MISR</u> MLDv2 Interrupt Status															00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MLDv2_ISR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MLDv2_ISR															
Type	W1C															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	MLDv2_ISR	MLDv2 Interrupt Status for entry 0~31 0: Not hit 1: Hit

000000D4		MISR_EXT1				MLDv2 Extension Interrupt Status I											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	MLDv2_ISR																	
Type	W1C																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	MLDv2_ISR																	
Type	W1C																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:0	MLDv2_ISR	MLDv2 Interrupt Status for entry 32~63 0: Not hit 1: Hit

000000E0				VAWD3				ACL Write Data III								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	WDATA																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	WDATA																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:0	WDATA	ACL Mask Table Write Data III

Bit(s)	Name	Description

000000E4	VAWD4				ACL Write Data IV												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	WDATA																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	WDATA																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:0	WDATA	ACL Mask Table Write Data IV

000000E8		VAWD5				ACL Write Data V											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	WDATA																	
Type	RW																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	WDATA																	
Type	RW																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:0	WDATA	ACL Mask Table Write Data V

000000EC	<u>VAWD6</u>				ACL Write Data VI												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	WDATA																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	WDATA																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:0	WDATA	ACL Mask Table Write Data VI

000000F0	<u>VAWD7</u>			ACL Write Data VII											00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	ACL Mask Table Write Data VII

000000F4 VAWD8 ACL Write Data VIII 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	WDATA															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	WDATA	ACL Mask Table Write Data VIII

00000100 PTC Port Trunking Control 0000FE00

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INFO_SEL														BUSY	
Type	RW														RO	
Reset	1	1	1	1	1	1	1								0	

Bit(s)	Name	Description
15:9	INFO_SEL	Information Control Bit Map The information used to assign conversations to ports. To apply the information, set corresponding bits to 1. BIT 0: Source Port BIT 1: MAC SA BIT 2: MAC DA BIT 3: IPv4/IPv6 SIP BIT 4: IPv4/IPv6 DIP BIT 5: TCP/UDP SPORT BIT 6: TCP/UDP DPORT
1	BUSY	Busy

Bit(s)	Name	Description
		0: IDLE
		1: BUSY

00000104 PTHS Port Trunking Algorithm Seed 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SEED															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
15:0	SEED	Seed

00000108 PTGCO Port Trunking Group Control 0 00001012

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		GRP_PORT1					GRP_PORT0				ACL_TNK	SA_LRN_PORT				LINK_DWN
Type		RW					RW				RW	RW				RO
Reset		0	0	1		0	0	0		0	0	1			1	0

Bit(s)	Name	Description
14:12	GRP_PORT1	Trunking Port 1 Set the trunking port of this group
10:8	GRP_PORT0	Trunking Port 0 Set the trunking port of this group
6	ACL_TNK	ACL Destination Port Trunking Enable Port Trunking for ACL forced destination port if the destination port is trunking port. 0: Disable 1: Enable
5:4	SA_LRN_PORT	Port Trunking Source MAC Address Learning Port Select the source port for MAC SA Learning if ingress port is in this trunking group. 2'b00: Ingress Port 2'b01: GRP_PORT0 2'b10: GRP_PORT1 2'b11: Reserved
1	LINK_DWN	Port Trunking Group Link Down Link down when all trunking ports link down Link up when one or more trunking ports link up

Bit(s)	Name	Description
0	EN	0: Link Up 1: Link Down Port Trunking Group Enable Enable/Disable this group 0: Disable 1: Enable

0000010C	PTGC1			Port Trunking Group Control 1												00004312	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		GRP_PORT1				GRP_PORT0				ACL_TNK	SA_LRN_PORT				LINK_DWN	EN	
Type		RW				RW				RW	RW				RO	RW	
Reset		1	0	0		0	1	1		0	0	1			1	0	

Bit(s)	Name	Description
14:12	GRP_PORT1	Trunking Port 1 Set the trunking port of this group
10:8	GRP_PORT0	Trunking Port 0 Set the trunking port of this group
6	ACL_TNK	ACL Destination Port Trunking Enable Port Trunking for ACL forced destination port if the destination port is trunking port. 0: Disable 1: Enable
5:4	SA_LRN_PORT	Port Trunking Source MAC Address Learning Port Select the source port for MAC SA Learning if ingress port is in this trunking group. 2'b00: Ingress Port 2'b01: GRP_PORT0 2'b10: GRP_PORT1 2'b11: Reserved
1	LINK_DWN	Port Trunking Group Link Down Link down when all trunking ports link down Link up when one or more trunking ports link up 0: Link Up 1: Link Down
0	EN	Port Trunking Group Enable Enable/Disable this group 0: Disable 1: Enable

00000110	<u>PTGC2</u>															Port Trunking Group Control 2															00006512														
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16																													
Name																																													

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GRP_PORT1					GRP_PORT0					ACL_TNK	SA_LRN_PORT			LINK_DWN	EN
Type	RW					RW					RW	RW			RO	RW
Reset		1	1	0		1	0	1		0	0	1			1	0

Bit(s)	Name	Description
14:12	GRP_PORT1	Trunking Port 1 Set the trunking port of this group
10:8	GRP_PORT0	Trunking Port 0 Set the trunking port of this group
6	ACL_TNK	ACL Destination Port Trunking Enable Port Trunking for ACL forced destination port if the destination port is trunking port. 0: Disable 1: Enable
5:4	SA_LRN_PORT	Port Trunking Source MAC Address Learning Port Select the source port for MAC SA Learning if ingress port is in this trunking group. 2'b00: Ingress Port 2'b01: GRP_PORT0 2'b10: GRP_PORT1 2'b11: Reserved
1	LINK_DWN	Port Trunking Group Link Down Link down when all trunking ports link down Link up when one or more trunking ports link up 0: Link Up 1: Link Down
0	EN	Port Trunking Group Enable Enable/Disable this group 0: Disable 1: Enable

00000114 PTGSC0 Port Trunking Group Security Control 0 0000FFF8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_SA_CNT															SA_CNT_EN
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1			0

Bit(s)	Name	Description
15:3	MAX_SA_CNT	SA Allowable Learning Number Maximum number of SA learned addresses for this trunking group when SA_CNT_EN is set.

Bit(s)	Name	Description
0	SA_CNT_EN	Enables the learned source MAC Address counter of this group 0: Disable 1: Enable

00000118 PTGSC1 Port Trunking Group Security Control 1 0000FFF8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_SA_CNT															SA_CNT_EN
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1			0

Bit(s)	Name	Description
15:3	MAX_SA_CNT	SA Allowable Learning Number Maximum number of SA learned addresses for this trunking group when SA_CNT_EN is set.
0	SA_CNT_EN	Enables the learned source MAC Address counter of this group 0: Disable 1: Enable

0000011C PTGSC2 Port Trunking Group Security Control 2 0000FFF8

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_SA_CNT															SA_CNT_EN
Type	RW															RW
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1			0

Bit(s)	Name	Description
15:3	MAX_SA_CNT	SA Allowable Learning Number Maximum number of SA learned addresses for this trunking group when SA_CNT_EN is set.
0	SA_CNT_EN	Enables the learned source MAC Address counter of this group 0: Disable 1: Enable

00000120 SPTC0 Port Trunking Table Control 84F0012C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	TBL1_GRP			TBL1_EN	TBL0_GRP			TBL0_EN	INFO_SEL				AGE_CNT			
Type	RW			RW	RW			RW	RW				RW			
Reset	1	0		0	0	1		0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AGE_CNT															
Type	RW															
Reset	0	0	0	0	0	0	0	1	0	0	1	0	1	1	0	0

Bit(s)	Name	Description
31:30	TBL1_GRP	Trunking Table 1 Group Selection Select trunking group to be serviced 2'b00: Group 0 2'b01: Group 1 2'b10: Group 2 2'b11: Reserved
28	TBL1_EN	Trunking Table 1 Enable 0: Disable 1: Enable
27:26	TBL0_GRP	Trunking Table 0 Group Selection Select trunking group to be serviced 2'b00: Group 0 2'b01: Group 1 2'b10: Group 2 2'b11: Reserved
24	TBL0_EN	Trunking Table 0 Enable 0: Disable 1: Enable
23:20	INFO_SEL	Trunking Table Information Control Bit Map The information used by table to assign conversations to ports. To apply the information, set corresponding bits in the bit map to 1. BIT 0: IPv4/IPv6 SIP BIT 1: IPv4/IPv6 DIP BIT 2: TCP/UDP SPORT BIT 3: TCP/UDP DPORT
19:0	AGE_CNT	Trunking Table Age Count This age count is recorded in the age timer field of the Trunking table for a new entry. The applied age timer is equal to AGE_CNT seconds.

2.10.2 ARL Port-Based Register

Module name: ARL_PORT Base address: (+0x0000)

Address	Name	Width	Register Function
00002000	<u>P0_SSC</u>	32	STP State Control of P0
00002004	<u>P0_PCR</u>	32	Port Control of P0
00002008	<u>P0_PIC</u>	32	Port IGMP Control of P0
0000200C	<u>P0_PSC</u>	32	Port Security Control of P0
00002010	<u>P0_PVC</u>	32	Port VLAN Control of P0
00002014	<u>P0_PPBV1</u>	32	Port-and-Protocol Based VLAN I of P0
00002018	<u>P0_PPBV2</u>	32	Port-and-Protocol Based VLAN II of P0
0000201C	<u>P0_BSR</u>	32	Broadcast Storm Rate Control of P0
00002020	<u>P0_STAG01</u>	32	STAG Index 0/1 of P0
00002024	<u>P0_STAG23</u>	32	STAG Index 2/3 of P0
00002028	<u>P0_STAG45</u>	32	STAG Index 4/5 of P0
0000202C	<u>P0_STAG67</u>	32	STAG Index 6/7 of P0
00002030	<u>P0_BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P0
00002034	<u>P0_BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P0
00002038	<u>P0_BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P0
00002040	<u>P0_UPW</u>	32	User Priority Weight of P0
00002044	<u>P0_PEM1</u>	32	User Priority Egress Mapping I of P0
00002048	<u>P0_PEM2</u>	32	User Priority Egress Mapping II of P0
0000204C	<u>P0_PEM3</u>	32	User Priority Egress Mapping III of P0
00002050	<u>P0_PEM4</u>	32	User Priority Egress Mapping IV of P0
00002100	<u>P1_SSC</u>	32	STP State Control of P1
00002104	<u>P1_PCR</u>	32	Port Control of P1
00002108	<u>P1_PIC</u>	32	Port IGMP Control of P1
0000210C	<u>P1_PSC</u>	32	Port Security Control of P1
00002110	<u>P1_PVC</u>	32	Port VLAN Control of P1
00002114	<u>P1_PPBV1</u>	32	Port-and-Protocol Based VLAN I of P1
00002118	<u>P1_PPBV2</u>	32	Port-and-Protocol Based VLAN II of P1
0000211C	<u>P1_BSR</u>	32	Broadcast Storm Rate Control of P1
00002120	<u>P1_STAG01</u>	32	STAG Index 0/1 of P1
00002124	<u>P1_STAG23</u>	32	STAG Index 2/3 of P1
00002128	<u>P1_STAG45</u>	32	STAG Index 4/5 of P1
0000212C	<u>P1_STAG67</u>	32	STAG Index 6/7 of P1
00002130	<u>P1_BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P1
00002134	<u>P1_BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P1
00002138	<u>P1_BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P1
00002140	<u>P1_UPW</u>	32	User Priority Weight of P1
00002144	<u>P1_PEM1</u>	32	User Priority Egress Mapping I of P1
00002148	<u>P1_PEM2</u>	32	User Priority Egress Mapping II of P1
0000214C	<u>P1_PEM3</u>	32	User Priority Egress Mapping III of P1
00002150	<u>P1_PEM4</u>	32	User Priority Egress Mapping IV of P1
00002200	<u>P2_SSC</u>	32	STP State Control of P2
00002204	<u>P2_PCR</u>	32	Port Control of P2
00002208	<u>P2_PIC</u>	32	Port IGMP Control of P2
0000220C	<u>P2_PSC</u>	32	Port Security Control of P2
00002210	<u>P2_PVC</u>	32	Port VLAN Control of P2
00002214	<u>P2_PPBV1</u>	32	Port-and-Protocol Based VLAN I of P2

00002218	<u>P2_PPBV2</u>	32	Port-and-Protocol Based VLAN II of P2
0000221C	<u>P2_BSR</u>	32	Broadcast Storm Rate Control of P2
00002220	<u>P2_STAG01</u>	32	STAG Index 0/1 of P2
00002224	<u>P2_STAG23</u>	32	STAG Index 2/3 of P2
00002228	<u>P2_STAG45</u>	32	STAG Index 4/5 of P2
0000222C	<u>P2_STAG67</u>	32	STAG Index 6/7 of P2
00002230	<u>P2_BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P2
00002234	<u>P2_BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P2
00002238	<u>P2_BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P2
00002240	<u>P2_UPW</u>	32	User Priority Weight of P2
00002244	<u>P2_PEM1</u>	32	User Priority Egress Mapping I of P2
00002248	<u>P2_PEM2</u>	32	User Priority Egress Mapping II of P2
0000224C	<u>P2_PEM3</u>	32	User Priority Egress Mapping III of P2
00002250	<u>P2_PEM4</u>	32	User Priority Egress Mapping IV of P2
00002300	<u>P3_SSC</u>	32	STP State Control of P3
00002304	<u>P3_PCR</u>	32	Port Control of P3
00002308	<u>P3_PIC</u>	32	Port IGMP Control of P3
0000230C	<u>P3_PSC</u>	32	Port Security Control of P3
00002310	<u>P3_PVC</u>	32	Port VLAN Control of P3
00002314	<u>P3_PPBV1</u>	32	Port-and-Protocol Based VLAN I of P3
00002318	<u>P3_PPBV2</u>	32	Port-and-Protocol Based VLAN II of P3
0000231C	<u>P3_BSR</u>	32	Broadcast Storm Rate Control of P3
00002320	<u>P3_STAG01</u>	32	STAG Index 0/1 of P3
00002324	<u>P3_STAG23</u>	32	STAG Index 2/3 of P3
00002328	<u>P3_STAG45</u>	32	STAG Index 4/5 of P3
0000232C	<u>P3_STAG67</u>	32	STAG Index 6/7 of P3
00002330	<u>P3_BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P3
00002334	<u>P3_BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P3
00002338	<u>P3_BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P3
00002340	<u>P3_UPW</u>	32	User Priority Weight of P3
00002344	<u>P3_PEM1</u>	32	User Priority Egress Mapping I of P3
00002348	<u>P3_PEM2</u>	32	User Priority Egress Mapping II of P3
0000234C	<u>P3_PEM3</u>	32	User Priority Egress Mapping III of P3
00002350	<u>P3_PEM4</u>	32	User Priority Egress Mapping IV of P3
00002400	<u>P4_SSC</u>	32	STP State Control of P4
00002404	<u>P4_PCR</u>	32	Port Control of P4
00002408	<u>P4_PIC</u>	32	Port IGMP Control of P4
0000240C	<u>P4_PSC</u>	32	Port Security Control of P4
00002410	<u>P4_PVC</u>	32	Port VLAN Control of P4
00002414	<u>P4_PPBV1</u>	32	Port-and-Protocol Based VLAN I of P4
00002418	<u>P4_PPBV2</u>	32	Port-and-Protocol Based VLAN II of P4
0000241C	<u>P4_BSR</u>	32	Broadcast Storm Rate Control of P4
00002420	<u>P4_STAG01</u>	32	STAG Index 0/1 of P4
00002424	<u>P4_STAG23</u>	32	STAG Index 2/3 of P4
00002428	<u>P4_STAG45</u>	32	STAG Index 4/5 of P4
0000242C	<u>P4_STAG67</u>	32	STAG Index 6/7 of P4
00002430	<u>P4_BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P4
00002434	<u>P4_BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P4
00002438	<u>P4_BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P4
00002440	<u>P4_UPW</u>	32	User Priority Weight of P4

00002444	<u>P4 PEM1</u>	32	User Priority Egress Mapping I of P4
00002448	<u>P4 PEM2</u>	32	User Priority Egress Mapping II of P4
0000244C	<u>P4 PEM3</u>	32	User Priority Egress Mapping III of P4
00002450	<u>P4 PEM4</u>	32	User Priority Egress Mapping IV of P4
00002500	<u>P5 SSC</u>	32	STP State Control of P5
00002504	<u>P5 PCR</u>	32	Port Control of P5
00002508	<u>P5 PIC</u>	32	Port IGMP Control of P5
0000250C	<u>P5 PSC</u>	32	Port Security Control of P5
00002510	<u>P5 PVC</u>	32	Port VLAN Control of P5
00002514	<u>P5 PPBV1</u>	32	Port-and-Protocol Based VLAN I of P5
00002518	<u>P5 PPBV2</u>	32	Port-and-Protocol Based VLAN II of P5
0000251C	<u>P5 BSR</u>	32	Broadcast Storm Rate Control of P5
00002520	<u>P5 STAG01</u>	32	STAG Index 0/1 of P5
00002524	<u>P5 STAG23</u>	32	STAG Index 2/3 of P5
00002528	<u>P5 STAG45</u>	32	STAG Index 4/5 of P5
0000252C	<u>P5 STAG67</u>	32	STAG Index 6/7 of P5
00002530	<u>P5 BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P5
00002534	<u>P5 BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P5
00002538	<u>P5 BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P5
00002540	<u>P5 UPW</u>	32	User Priority Weight of P5
00002544	<u>P5 PEM1</u>	32	User Priority Egress Mapping I of P5
00002548	<u>P5 PEM2</u>	32	User Priority Egress Mapping II of P5
0000254C	<u>P5 PEM3</u>	32	User Priority Egress Mapping III of P5
00002550	<u>P5 PEM4</u>	32	User Priority Egress Mapping IV of P5
00002554	<u>P5 BSR_EXT4</u>	32	Broadcast Storm Rate Control IV of P5
00002558	<u>P5 BSR_EXT5</u>	32	Broadcast Storm Rate Control V of P5
00002600	<u>P6 SSC</u>	32	STP State Control of P6
00002604	<u>P6 PCR</u>	32	Port Control of P6
00002608	<u>P6 PIC</u>	32	Port IGMP Control of P6
0000260C	<u>P6 PSC</u>	32	Port Security Control of P6
00002610	<u>P6 PVC</u>	32	Port VLAN Control of P6
00002614	<u>P6 PPBV1</u>	32	Port-and-Protocol Based VLAN I of P6
00002618	<u>P6 PPBV2</u>	32	Port-and-Protocol Based VLAN II of P6
0000261C	<u>P6 BSR</u>	32	Broadcast Storm Rate Control of P6
00002620	<u>P6 STAG01</u>	32	STAG Index 0/1 of P6
00002624	<u>P6 STAG23</u>	32	STAG Index 2/3 of P6
00002628	<u>P6 STAG45</u>	32	STAG Index 4/5 of P6
0000262C	<u>P6 STAG67</u>	32	STAG Index 6/7 of P6
00002630	<u>P6 BSR_EXT1</u>	32	Broadcast Storm Rate Control I of P6
00002634	<u>P6 BSR_EXT2</u>	32	Broadcast Storm Rate Control II of P6
00002638	<u>P6 BSR_EXT3</u>	32	Broadcast Storm Rate Control III of P6
00002640	<u>P6 UPW</u>	32	User Priority Weight of P6
00002644	<u>P6 PEM1</u>	32	User Priority Egress Mapping I of P6
00002648	<u>P6 PEM2</u>	32	User Priority Egress Mapping II of P6
0000264C	<u>P6 PEM3</u>	32	User Priority Egress Mapping III of P6
00002650	<u>P6 PEM4</u>	32	User Priority Egress Mapping IV of P6
00002654	<u>P6 BSR_EXT4</u>	32	Broadcast Storm Rate Control IV of P6
00002658	<u>P6 BSR_EXT5</u>	32	Broadcast Storm Rate Control V of P6

00002000 P0_SSC STP State Control of P0 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REVO	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
11:10	FID5_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
9:8	FID4_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
7:6	FID3_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
5:4	FID2_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
3:2	FID1_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
1:0	FID0_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)

Bit(s)	Name	Description

00002004 P0_PCR Port Control of P0 00FF2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	RW	RW	RW		RW	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding enable 0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	Port-based ACL Enable 0: Bypass the ACL Table. 1: Look up the ACL Table and take corresponding actions.
9	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	Port Rx Mirror Enable All frames received from this port are copied to the mirror port.

Bit(s)	Name	Description
		[NOTE] Multi-port support is possible.
		0: Disable
		1: Enable
7	ACL_MIR	ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port 1'b0: Frame is processed according to PORT_VLAN. 1'b1: VLAN mismatched frame is copied to MIRROR port.
1:0	PORT_VLAN	Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port do not belong to the VLAN member. Discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002008 P0_PIC Port IGMP Control of P0 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0												IGMP_MIR	IGMP_MIS		
Type	RO												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR	MLD_H_W_LEA	IGMP_HW_LEAVE	REV1	IPM_22_44	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_S_QRY_EN	IGMP_S_QRY_EN	MLD_G_QRY_EN	IGMP_G_QRY_EN	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REV0	Reserved
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port.

Bit(s)	Name	Description
		[NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed from the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed from the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	Reserved
10	IPM_2244	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable

Bit(s)	Name	Description
		Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00::/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD-specific query message does not refresh the IP multicast table. 1: This port is capable of recognizing the MLD-specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP-specific query message does not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP-specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000200C				P0_PSC				Port Security Control of P0								000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	SA_LRN_CNT												MAC_SA_LRN						
Type	RO												RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK			
Type	RW								RW		RW	RW	RW		RW	RW			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Set the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table

Bit(s)	Name	Description
7:6	REVO	12'hFFF: SA Learning without limitation
5	SA_CNT_EN	Reserved SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and is not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or the received frames that are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002010	P0_PVC					Port VLAN Control of P0											810000C0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	STAG_VPID																	
Type	RW																	
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	DIS_PV ID	FORCE _PVID	BC_LKY V_EN	REVO	PT_OP TION	EG_TAG			VLAN_ATTR		PORT_ STAG	IPM_LK YV_EN	MC_LK YV_EN	UC_LKY V_EN	ACC_FRM			
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW			
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0		

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames.

Bit(s)	Name	Description
14	FORCE_PVID	1: Keep VID=0 for priority-tagged frames. Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame.
13	BC_LKYV_EN	1: Force the replacement of VID with PVID. Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved
11	PT_OPTION	Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002014	P0_PPBV1			Port-and-Protocol Based VLAN I of P0												00010001
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REVO	G1_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002018 P0_PPBV2 Port-and-Protocol Based VLAN II of P0 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

0000201C P0_BSR Broadcast Storm Rate Control of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002020	<u>P0_STAG01</u>				STAG Index 0/1 of P0												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	REVO								VID1											
Type	RO								RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	VID1				VID0															
Type	RW				RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:24	REVO	Reserved

Bit(s)	Name	Description
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002024 P0_STAG23 STAG Index 2/3 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

00002028 P0_STAG45 STAG Index 4/5 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000202C P0_STAG67 STAG Index 6/7 of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002030 P0_BSR_EXT1 Broadcast Storm Rate Control I of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps

Bit(s)	Name	Description
8'h1: (1* STORM_UNIT) packets or bps		

00002034 P0_BSR_EXT2 Broadcast Storm Rate Control II of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

Bit(s)	Name	Description

00002038 P0_BSR_EXT3 Broadcast Storm Rate Control III of P0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002040 **P0_UPW** **User Priority Weight of P0** **00234567**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002044 **P0_PEM1** **User Priority Egress Mapping I of P0** **10080480**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC TX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002048 **P0_PEM2** **User Priority Egress Mapping II of P0** **36D82250**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000204C P0_PEM3 User Priority Egress Mapping III of P0 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002050 P0_PEM4 User Priority Egress Mapping IV of P0 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	REV1	TAG_PRI_6				QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW				RW			RW			RW					
Reset	0	1	1	0		1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

00002100 P1_SSC STP State Control of P1 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
11:10	FID5_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
9:8	FID4_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
7:6	FID3_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP)

Bit(s)	Name	Description
5:4	FID2_PST	2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP) (Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP)
3:2	FID1_PST	2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP) (Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP)
1:0	FID0_PST	2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP) (Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)

00002104 P1_PCR Port Control of P1 00FF2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	RW	RW	RW		RW	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DS_CP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding enable 0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved

Bit(s)	Name	Description
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	Port-based ACL Enable 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	Port Rx Mirror Enable All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port 1'b0: Frame is processed according to PORT_VLAN. 1'b1: VLAN mismatched frame is copied to MIRROR port.
1:0	PORT_VLAN	Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. Discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO												IGMP_MIR	IGMP_MIS		
Type	RO												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REVO	Reserved
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	Reserved
10	IPM_2244	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table.

Bit(s)	Name	Description
9	IPM_33	1: This frame is regarded as an IP multicast frame and search IGMP table. IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table.
8	IPM_01	1: This frame is regarded as IP multicast frame and search IGMP table. IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table.
7	MLD2_JOIN_EN	1: This frame is regarded as IP multicast frame and search IGMP table. MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000210C	P1_PSC				Port Security Control of P1								000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK
Type	RW								RW		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	Reserved
5	SA_CNT_EN	SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002110 P1_PVC Port VLAN Control of P1 810000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PV ID	FORCE _PVID	BC_LKY V_EN	REV0	PT_OP TION	EG_TAG			VLAN_ATTR		PORT_ STAG	IPM_LK YV_EN	MC_LK YV_EN	UC_LKY V_EN	ACC_FRM	
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW	

Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID.
13	BC_LKYV_EN	Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved
11	PT_OPTION	Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type

Bit(s)	Name	Description
		2'b00: Admit All frames
		2'b01: Admit Only VLAN-tagged frames
		2'b10: Admit only untagged or priority-tagged frames.
		2'b11: Reserved

00002114 P1_PPBV1 Port-and-Protocol Based VLAN I of P1 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002118 P1_PPBV2 Port-and-Protocol Based VLAN II of P1 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

Bit(s)	Name	Description

0000211C	P1_BSR							Broadcast Storm Rate Control of P1							00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002120 P1_STAG01 STAG Index 0/1 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002124 P1_STAG23 STAG Index 2/3 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

00002128 P1_STAG45 STAG Index 4/5 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000212C P1_STAG67 STAG Index 6/7 of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002130 P1_BSR_EXT1 Broadcast Storm Rate Control I of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps

Bit(s)	Name	Description
23:16	STORM_1G	2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps 1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002134	P1_BSR_EXT2						Broadcast Storm Rate Control II of P1								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G									
Type	RW	RW	RW	RW	RW	RW	RW		RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	STORM_100M								STORM_10M									
Type	RW								RW									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps

Bit(s)	Name	Description
23:16	STORM_1G	2'b11: 4 K packets or 4 Mbps 1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002138 P1_BSR_EXT3 Broadcast Storm Rate Control III of P1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps

Bit(s)	Name	Description
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002140 P1_UPW User Priority Weight of P1 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002144 P1_PEM1 User Priority Egress Mapping I of P1 10080480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC TX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002148 P1_PEM2 User Priority Egress Mapping II of P1 36D82250

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000214C P1_PEM3 User Priority Egress Mapping III of P1 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping

Bit(s)	Name	Description
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002150 P1_PEM4 User Priority Egress Mapping IV of P1 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_6			QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

00002200 P2_SSC STP State Control of P2 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST	FID6_PST	FID5_PST	FID4_PST	FID3_PST	FID2_PST	FID1_PST	FID0_PST								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP)

Bit(s)	Name	Description
11:10	FID5_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
9:8	FID4_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
7:6	FID3_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
5:4	FID2_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
3:2	FID1_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
1:0	FID0_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)

00002204		P2_PCR		Port Control of P2												00FF2000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX								
Type	RW	RW	RW		RW	RW			RW								
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	REV2			UP2DS_CP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN		
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW		
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding enable

Bit(s)	Name	Description
		0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority 0: Disable 1: Enable
10	ACL_EN	Port-based ACL Enable 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	Port Rx Mirror Enable All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port

Bit(s)	Name	Description
1:0	PORT_VLAN	1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port. Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002208	P2_PIC			Port IGMP Control of P2										00008000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	REVO												IGMP_MIR	IGMP_MIS			
Type	RO												RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_22_44	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN	
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:20	REVO	Reserved
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out)

Bit(s)	Name	Description
		1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	Reserved
10	IPM_2244	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.

Bit(s)	Name	Description
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000220C		P2_PSC				Port Security Control of P2								000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	SA_LRN_CNT												MAC_SA_LRN				
Type	RO												RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK	
Type	RW								RW		RW	RW	RW		RW	RW	
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REVO	Reserved
5	SA_CNT_EN	SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock.

Bit(s)	Name	Description
0	RX_PORT_LOCK	0: Transmit authorized. 1: Disable frame transmission. Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002210	P2_PVC			Port VLAN Control of P2										810000C0		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PV_ID	FORCE_PVID	BC_LKY_V_EN	REVO	PT_OP_TION	EG_TAG			VLAN_ATTR		PORT_STAG	IPM_LK_YV_EN	MC_LK_YV_EN	UC_LKY_V_EN	ACC_FRM	
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID.
13	BC_LKYV_EN	Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
11	PT_OPTION	
10:8	EG_TAG	
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port

Bit(s)	Name	Description
5	PORT_STAG	2'b10: Translation port 2'b11: Transparent port Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002214	<u>P2_PPBV1</u>			Port-and-Protocol Based VLAN I of P2												00010001	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	G1_PORT_PRI			REV0	G1_PORT_VID												
Type	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	G0_PORT_PRI			REV1	G0_PORT_VID												
Type	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002218	P2_PPBV2	Port-and-Protocol Based VLAN II of P2	00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

0000221C P2_BSR Broadcast Storm Rate Control of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us

Bit(s)	Name	Description
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002220 P2_STAG01 STAG Index 0/1 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002224 P2_STAG23 STAG Index 2/3 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

Bit(s)	Name	Description

00002228 P2_STAG45 STAG Index 4/5 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000222C P2_STAG67 STAG Index 6/7 of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002230 P2_BSR_EXT1 Broadcast Storm Rate Control I of P2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002234		P2_BSR_EXT2		Broadcast Storm Rate Control II of P2								00000000					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G								
Type	RW	RW	RW	RW	RW	RW	RW		RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	STORM_100M								STORM_10M								
Type	RW								RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression

Bit(s)	Name	Description
		0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002238	P2_BSR_EXT3			Broadcast Storm Rate Control III of P2										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period)

Bit(s)	Name	Description
30	STRM_BC_INC	1: Rate-based Broadcast Storm Included 0: Exclude BC frame
29	STRM_MC_INC	1: Include BC frame Unknown Multicast Storm Included 0: Exclude MC frame
28	STRM_UC_INC	1: Include MC frame Unknown Unicast Storm Included 0: Exclude UC frame
27	STRM_DROP	1: Include UC frame Broadcast Storm Suppression enabled 0: BC Storm detection only
26	STRM_PERD	1: Enable packet drop when BC storm is detected Broadcast Storm Detection Signal Period 0: One second
25:24	STRM_UNIT	1: 125us Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002240 **P2_UPW** User Priority Weight of P2 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.

Bit(s)	Name	Description
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002244 P2_PEM1 User Priority Egress Mapping I of P2 10080480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC TX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002248 P2_PEM2 User Priority Egress Mapping II of P2 36D82250

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved

Bit(s)	Name	Description
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000224C P2_PEM3 User Priority Egress Mapping III of P2 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002250 P2_PEM4 User Priority Egress Mapping IV of P2 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_6			QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

Bit(s)	Name	Description

00002300	P3_SSC				STP State Control of P3										0000FFFF			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	REVO																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST			
Type	RW		RW		RW		RW		RW		RW		RW		RW			
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1		

Bit(s)	Name	Description
31:16	REVO	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
11:10	FID5_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
9:8	FID4_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
7:6	FID3_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
5:4	FID2_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
3:2	FID1_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
1:0	FID0_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP)

Bit(s)	Name	Description
2'b01:		Listening (STP) / Discard (RSTP)
2'b10:		Learning (STP) / Learning (RSTP)
2'b11:		Forwarding (STP) / Forwarding (RSTP)

00002304 P3_PCR Port Control of P3 00FF2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	RW	RW	RW		RW	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding Enable 0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	Port-based ACL Enable 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable

Bit(s)	Name	Description
8	PORT_RX_MIR	1: Enable Port Rx Mirror Enable All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable
7	ACL_MIR	1: Enable ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable
6:4	MIS_PORT_FW	1: Enable ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002308				P3_PIC		Port IGMP Control of P3										00008000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	REV0												IGMP_MIR	IGMP_MIS					
Type	RO												RW	RW					
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_22_44	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN			
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:20	REV0	Reserved

Bit(s)	Name	Description
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable

Bit(s)	Name	Description
		Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00::/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000230C				P3_PSC				Port Security Control of P3								000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	SA_LRN_CNT												MAC_SA_LRN						
Type	RO												RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK			
Type	RW								RW		RW	RW	RW		RW	RW			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table

Bit(s)	Name	Description
7:6	REVO	12'hFFF: SA Learning without limitation
5	SA_CNT_EN	Reserved SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002310		P3_PVC				Port VLAN Control of P3										810000C0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	STAG_VPID																
Type	RW																
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	DIS_PV_ID	FORCE_PVID	BC_LKY_V_EN	REVO	PT_OPTION	EG_TAG			VLAN_ATTR		PORT_STAG	IPM_LKY_V_EN	MC_LKY_V_EN	UC_LKY_V_EN	ACC_FRM		
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames.

Bit(s)	Name	Description
14	FORCE_PVID	1: Keep VID=0 for priority-tagged frames. Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame.
13	BC_LKYV_EN	1: Force the replacement of VID with PVID. Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved
11	PT_OPTION	Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002314	P3_PPBV1			Port-and-Protocol Based VLAN I of P3												00010001	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	G1_PORT_PRI			REVO	G1_PORT_VID												
Type	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002318 P3_PPBV2 Port-and-Protocol Based VLAN II of P3 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

0000231C P3_BSR Broadcast Storm Rate Control of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002320 P3 STAG01 STAG Index 0/1 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved

Bit(s)	Name	Description
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002324 P3_STAG23 STAG Index 2/3 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

00002328 P3_STAG45 STAG Index 4/5 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000232C P3_STAG67 STAG Index 6/7 of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002330 P3_BSR_EXT1 Broadcast Storm Rate Control I of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps

Bit(s)	Name	Description
8'h1: (1* STORM_UNIT) packets or bps		

00002334 P3_BSR_EXT2 Broadcast Storm Rate Control II of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

Bit(s)	Name	Description

00002338 P3_BSR_EXT3 Broadcast Storm Rate Control III of P3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002340 **P3_UPW** User Priority Weight of P3 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002344 **P3_PEM1** User Priority Egress Mapping I of P3 10080480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC TX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002348 **P3_PEM2** User Priority Egress Mapping II of P3 36D82250

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000234C P3_PEM3 User Priority Egress Mapping III of P3 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002350 P3_PEM4 User Priority Egress Mapping IV of P3 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	REV1	TAG_PRI_6				QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW				RW			RW			RW					
Reset	0	1	1	0		1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

00002400 P4_SSC STP State Control of P4 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
11:10	FID5_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
9:8	FID4_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
7:6	FID3_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP)

Bit(s)	Name	Description
5:4	FID2_PST	2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP) (Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP)
3:2	FID1_PST	2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP) (Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP)
1:0	FID0_PST	2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP) (Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)

00002404 P4_PCR Port Control of P4 00FF2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	RW	RW	RW		RW	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DS_CP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding enable 0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved

Bit(s)	Name	Description
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	Port-based ACL Enable 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	Port Rx Mirror Enable All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002408

P4_PIC

Port IGMP Control of P4

00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO												IGMP_MIR	IGMP_MIS		
Type	RO												RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REVO	Reserved
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table.
10	IPM_2244	

Bit(s)	Name	Description
9	IPM_33	1: This frame is regarded as an IP multicast frame and search IGMP table. IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table.
8	IPM_01	1: This frame is regarded as IP multicast frame and search IGMP table. IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table.
7	MLD2_JOIN_EN	1: This frame is regarded as IP multicast frame and search IGMP table. MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000240C	P4_PSC				Port Security Control of P4								000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SA_LRN_CNT												MAC_SA_LRN			
Type	RO												RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK
Type	RW								RW		RW	RW	RW		RW	RW
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REV0	Reserved
5	SA_CNT_EN	SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002410 P4_PVC Port VLAN Control of P4 810000C0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PV ID	FORCE _PVID	BC_LKY V_EN	REV0	PT_OP TION	EG_TAG			VLAN_ATTR		PORT_ STAG	IPM_LK YV_EN	MC_LK YV_EN	UC_LKY V_EN	ACC_FRM	
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW	

Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID.
13	BC_LKYV_EN	Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved
11	PT_OPTION	Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type

Bit(s)	Name	Description
		2'b00: Admit All frames
		2'b01: Admit Only VLAN-tagged frames
		2'b10: Admit only untagged or priority-tagged frames.
		2'b11: Reserved

00002414 P4_PPBV1 Port-and-Protocol Based VLAN I of P4 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002418 P4_PPBV2 Port-and-Protocol Based VLAN II of P4 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

Bit(s)	Name	Description

0000241C P4_BSR Broadcast Storm Rate Control of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002420 P4_STAG01 STAG Index 0/1 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002424 P4_STAG23 STAG Index 2/3 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

00002428 P4_STAG45 STAG Index 4/5 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000242C P4_STAG67 STAG Index 6/7 of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002430 P4_BSR_EXT1 Broadcast Storm Rate Control I of P4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps

Bit(s)	Name	Description
		2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002434	P4_BSR_EXT2			Broadcast Storm Rate Control II of P4										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps

Bit(s)	Name	Description
23:16	STORM_1G	2'b11: 4 K packets or 4 Mbps 1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002438	P4_BSR_EXT3			Broadcast Storm Rate Control III of P4										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps

Bit(s)	Name	Description
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002440 P4_UPW User Priority Weight of P4 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002444 P4_PEM1 User Priority Egress Mapping I of P4 10080480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC TX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC RX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002448 P4_PEM2 User Priority Egress Mapping II of P4 36D82250

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000244C P4_PEM3 User Priority Egress Mapping III of P4 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping

Bit(s)	Name	Description
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002450 P4_PEM4 User Priority Egress Mapping IV of P4 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_6			QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

00002500 P5_SSC STP State Control of P5 0000FFFF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST	FID6_PST	FID5_PST	FID4_PST	FID3_PST	FID2_PST	FID1_PST	FID0_PST								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REV0	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP)

Bit(s)	Name	Description
11:10	FID5_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
9:8	FID4_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
7:6	FID3_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
5:4	FID2_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
3:2	FID1_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)
1:0	FID0_PST	2'b01: Listening (STP) / Discard (RSTP)
		2'b10: Learning (STP) / Learning (RSTP)
		2'b11: Forwarding (STP) / Forwarding (RSTP)
		(Rapid) Spanning Tree Protocol Port State
		2'b00: Disable (STP) / Discard (RSTP)

00002504		P5_PCR		Port Control of P5												00FF2000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX								
Type	RW	RW	RW		RW	RW			RW								
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	REV2			UP2DS_CP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN		
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW		
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding enable

Bit(s)	Name	Description
		0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority. 0: Disable 1: Enable
10	ACL_EN	Port-based ACL Enable 0: Bypass the ACL Table. 1: Lookup the ACL Table and take the corresponding actions.
9	PORT_TX_MIR	Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
8	PORT_RX_MIR	Port Rx Mirror Enable All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable 1: Enable
7	ACL_MIR	ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable 1: Enable
6:4	MIS_PORT_FW	ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port

Bit(s)	Name	Description
1:0	PORT_VLAN	1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port. Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames once if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002508	P5_PIC			Port IGMP Control of P5										00008000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	REVO												IGMP_MIR	IGMP_MIS			
Type	RO												RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	ROBUST_VAR		MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM22_44	IPM33	IPM01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN	
Type	RW		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:20	REVO	Reserved
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out)

Bit(s)	Name	Description
		1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table. 1: This frame is regarded as IP multicast frame and search IGMP table.
7	MLD2_JOIN_EN	MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00:/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.

Bit(s)	Name	Description
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000250C		P5_PSC		Port Security Control of P5										000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	SA_LRN_CNT												MAC_SA_LRN				
Type	RO												RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK	
Type	RW								RW		RW	RW	RW		RW	RW	
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REVO	Reserved
5	SA_CNT_EN	SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frames whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock.

Bit(s)	Name	Description
0	RX_PORT_LOCK	0: Transmit authorized. 1: Disable frame transmission. Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002510	P5_PVC		Port VLAN Control of P5												810000C0	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STAG_VPID															
Type	RW															
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DIS_PV_ID	FORCE_PVID	BC_LKY_V_EN	REVO	PT_OP_TION	EG_TAG			VLAN_ATTR		PORT_STAG	IPM_LK_YV_EN	MC_LK_YV_EN	UC_LKY_V_EN	ACC_FRM	
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID.
13	BC_LKYV_EN	Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
11	PT_OPTION	
10:8	EG_TAG	
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port

Bit(s)	Name	Description
5	PORT_STAG	2'b10: Translation port 2'b11: Transparent port Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames. 2'b11: Reserved

00002514	<u>P5_PPBV1</u>			Port-and-Protocol Based VLAN I of P5												00010001	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	G1_PORT_PRI			REV0	G1_PORT_VID												
Type	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	G0_PORT_PRI			REV1	G0_PORT_VID												
Type	RW			RW	RW												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002518	P5_PPBV2	Port-and-Protocol Based VLAN II of P5	00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

0000251C P5_BSR Broadcast Storm Rate Control of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us

Bit(s)	Name	Description
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002520 P5_STAG01 STAG Index 0/1 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID1							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002524 P5_STAG23 STAG Index 2/3 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

Bit(s)	Name	Description

00002528 P5_STAG45 STAG Index 4/5 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000252C P5_STAG67 STAG Index 6/7 of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002530 P5_BSR_EXT1 Broadcast Storm Rate Control I of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002534	P5_BSR_EXT2			Broadcast Storm Rate Control II of P5										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression

Bit(s)	Name	Description
		0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002538 P5_BSR_EXT3 Broadcast Storm Rate Control III of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period)

Bit(s)	Name	Description
30	STRM_BC_INC	1: Rate-based Broadcast Storm Included 0: Exclude BC frame
29	STRM_MC_INC	1: Include BC frame Unknown Multicast Storm Included 0: Exclude MC frame
28	STRM_UC_INC	1: Include MC frame Unknown Unicast Storm Included 0: Exclude UC frame
27	STRM_DROP	1: Include UC frame Broadcast Storm Suppression enabled 0: BC Storm detection only
26	STRM_PERD	1: Enable packet drop when BC storm is detected Broadcast Storm Detection Signal Period 0: One second
25:24	STRM_UNIT	1: 125us Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002540 P5_UPW User Priority Weight of P5 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.

Bit(s)	Name	Description
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002544 P5_PEM1 User Priority Egress Mapping I of P5 10080480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC TX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002548 P5_PEM2 User Priority Egress Mapping II of P5 36D82250

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved

Bit(s)	Name	Description
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000254C P5_PEM3 User Priority Egress Mapping III of P5 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002550 P5_PEM4 User Priority Egress Mapping IV of P5 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_6			QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

Bit(s)	Name	Description

00002554 P5_BSR_EXT4 Broadcast Storm Rate Control IV of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STORM_2P5G_EXT3								STORM_2P5G_EXT2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_2P5G_EXT1								STORM_2P5G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	STORM_2P5G_EXT3	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
23:16	STORM_2P5G_EXT2	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_2P5G_EXT1	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_2P5G	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002558 P5_BSR_EXT5 Broadcast Storm Rate Control V of P5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO												STRM_UNIT_1_EXT3	STRM_UNIT_1_EXT2	STRM_UNIT_1_EXT1	STRM_UNIT_1
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	REVO	Reserved
3	STRM_UNIT_1_EXT3	Broadcast Storm Suppression

Bit(s)	Name	Description
2	STRM_UNIT_1_EXT2	1'b1: 16 K packets or 16 Mbps Broadcast Storm Suppression
1	STRM_UNIT_1_EXT1	1'b1: 16 K packets or 16 Mbps Broadcast Storm Suppression
0	STRM_UNIT_1	1'b1: 16 K packets or 16 Mbps Broadcast Storm Suppression

00002600	P6_SSC		STP State Control of P6												0000FFFF	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	FID7_PST		FID6_PST		FID5_PST		FID4_PST		FID3_PST		FID2_PST		FID1_PST		FID0_PST	
Type	RW		RW		RW		RW		RW		RW		RW		RW	
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
31:16	REVO	Reserved
15:14	FID7_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
13:12	FID6_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
11:10	FID5_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
9:8	FID4_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
7:6	FID3_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
5:4	FID2_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)

Bit(s)	Name	Description
3:2	FID1_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)
1:0	FID0_PST	(Rapid) Spanning Tree Protocol Port State 2'b00: Disable (STP) / Discard (RSTP) 2'b01: Listening (STP) / Discard (RSTP) 2'b10: Learning (STP) / Learning (RSTP) 2'b11: Forwarding (STP) / Forwarding (RSTP)

00002604 P6_PCR Port Control of P6 00FF2000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	MLDv2_EN	EG_TAG		REV1	PORT_PRI			PORT_MATRIX							
Type	RW	RW	RW		RW	RW			RW							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2			UP2DSCP_EN	UP2TAG_EN	ACL_EN	PORT_TX_MIR	PORT_RX_MIR	ACL_MIR	MIS_PORT_FW			REV3	VLAN_MIS	PORT_VLAN	
Type	RW			RW	RW	RW	RW	RW	RW	RW			RW	RW	RW	
Reset	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30	MLDv2_EN	IPv6 MLDv2 source address multicast forwarding enable 0: Disable 1: Enable
29:28	EG_TAG	Port-Based Egress VLAN Tag Attribution 2'b00: Untagged 2'b01: Swap 2'b10: Tagged 2'b11: Stack
27	REV1	Reserved
26:24	PORT_PRI	Port-based User Priority User priority for the ingress port
23:16	PORT_MATRIX	Port Matrix Member The legacy port VLAN function. Each bit indicates the permissible egress ports. This function can work with 802.1Q function to decide the last port member. NOTE: The final and effective port member should exclude the received port.
15:13	REV2	Reserved
12	UP2DSCP_EN	User Priority to DSCP Enable Replace DSCP according to user priority. 0: Disable 1: Enable
11	UP2TAG_EN	User Priority to Tag Enable Replace 802.Q priority by user priority. 0: Disable

Bit(s)	Name	Description
10	ACL_EN	1: Enable Port-based ACL Enable 0: Bypass the ACL Table.
9	PORT_TX_MIR	1: Lookup the ACL Table and take the corresponding actions. Port Tx Mirror Enable All frames transmitted from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable
8	PORT_RX_MIR	1: Enable Port Rx Mirror Enable All frames received from this port are copied to the mirror port. [NOTE] Multi-port support is possible. 0: Disable
7	ACL_MIR	1: Enable ACL Mismatch to Mirror Port Frames are copied to Mirror port when the ACL table is enabled and the frame does not match any ACL rule. 0: Disable
6:4	MIS_PORT_FW	1: Enable ACL Mismatch TO_CPU Forward Frame port forwarding when ACL table is enabled and the frame is mismatched 3'b0xx: System default (disabled) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
3	REV3	Reserved
2	VLAN_MIS	VLAN Mismatch to Mirror Port 1'b0: Frame processed according to PORT_VLAN. 1'b1: VLAN mismatched frame copied to MIRROR port.
1:0	PORT_VLAN	Port-based VLAN Mechanism Select 2'b00: Port Matrix Mode. Frames are forwarded by the Port Matrix Member. 2'b01: Fallback Mode. Forward received frames with ingress ports that do not belong to the VLAN member. Each frame whose VID is not listed on the VLAN table is forwarded based on the Port Matrix member. 2'b10: Check Mode. Forward received frames whose ingress port does not belong to the VLAN member. But, discard frames if VID is missed on the VLAN table. 2'b11: Security Mode. Enable VLAN security and discard any frame due to ingress membership violation or VID missed on the VLAN table.

00002608				Port IGMP Control of P6										00008000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	REVO												IGMP_MIR	IGMP_MIS			
Type	RO												RW	RW			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	ROBUST_VAR	MLD_HW_LEAVE	IGMP_HW_LEAVE	REV1	IPM_2244	IPM_33	IPM_01	MLD2_JOIN_EN	IGMP3_JOIN_EN	MLD_JOIN_EN	IGMP_JOIN_EN	MLD_SQRY_EN	IGMP_SQRY_EN	MLD_GQRY_EN	IGMP_GQRY_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:20	REVO	Reserved
19	IGMP_MIR	IP Multicast IGMP Table Mismatch to Mirror Port Copy IP multicast frames with an IGMP table mismatch to the mirror port. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 0: Disable 1: Frame copied to Mirror port
18:16	IGMP_MIS	IP Multicast "TO_CPU" Forwarding Select how to forward IP multicast frames when the IGMP table is mismatched. [NOTE] This control register is valid only if PSR.IGMP_EN or MLD_EN is set on a per-port basis. 3'b0xx: System default (By MFC.UNM_FFP) 3'b100: System default and CPU port excluded 3'b101: System default and CPU port included 3'b110: CPU port only (As long as the ingress port is not the CPU port. If the ingress port is the CPU port, the system default and CPU port are excluded.) 3'b111: Frame dropped
15:14	ROBUST_VAR	Robustness Variable Define the number of times an IGMP report message may be lost consecutively. 0: Unlimited (No Age out) 1: One time 2: Two times (default) 3: Three times
13	MLD_HW_LEAVE	MLD HW Leave Enable Enable HW MLD Done snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
12	IGMP_HW_LEAVE	IGMP HW Leave Enable Enable HW IGMP Leave snooping and fast leave. The corresponding incoming port will be removed on the specific group address without a group-specific query. 0: Disable 1: Enable
11	REV1	
10	IPM_2244	IP Multicast frame for DIP is Class D:224.x.x.x to 239.x.x.x 0: This frame is regarded as a normal multicast and search ADDR Table. 1: This frame is regarded as an IP multicast frame and search IGMP table.
9	IPM_33	IP Multicast frame for MAC DA is 33-33-xx-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR table. 1: This frame is regarded as IP multicast frame and search IGMP table.
8	IPM_01	IP Multicast frame for MAC DA is 01-00-5E-xx-xx-xx 0: This frame is regarded as normal multicast and search ADDR Table.

Bit(s)	Name	Description
7	MLD2_JOIN_EN	1: This frame is regarded as IP multicast frame and search IGMP table. MLD v2 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
6	IGMP3_JOIN_EN	IGMP v3 HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically for the specific Record Type -IS_EX(), TO_EX(). 0: Disable 1: Enable
5	MLD_JOIN_EN	MLD Snooping HW Join Enable 0: MLD message and multicast IPv6 frame is regarded as a general multicast frame. 1: This port is capable of recognizing the MLD message and multicast IPv6 frames (FF00::/8).
4	IGMP_JOIN_EN	IGMP Snooping HW Join Enable Enable HW IGMP snooping. Group Address will be learned and added to the ADDR Table automatically. 0: Disable 1: Enable
3	MLD_SQRY_EN	MLD HW Specific Query Enable 0: MLD specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD specific query message to refresh the specific multicast member.
2	IGMP_SQRY_EN	IGMP HW Specific Query Enable 0: IGMP specific query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP specific query message to refresh the specific multicast member.
1	MLD_GQRY_EN	MLD HW General Query Enable 0: MLD general query message will not refresh the IP multicast table. 1: This port is capable of recognizing the MLD general query message to refresh the multicast member.
0	IGMP_GQRY_EN	IGMP HW General Query Enable 0: IGMP general Query message will not refresh the IP multicast table. 1: This port is capable of recognizing the IGMP general query message to refresh the multicast member.

0000260C				P6_PSC				Port Security Control of P6								000FFF00			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	SA_LRN_CNT												MAC_SA_LRN						
Type	RO												RW						
Reset	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	MAC_SA_LRN								REV0		SA_CN T_EN	SA_DIS	SA_LOCK		TX_PO RT_LOC K	RX_PO RT_LO CK			
Type	RW								RW		RW	RW	RW		RW	RW			
Reset	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:20	SA_LRN_CNT	Learned Source Address Number
19:8	MAC_SA_LRN	Rx SA Allowable Learning Number Sets the maximum number of SA learned addresses when SA_CNT_EN is set. 12'h0: Disable SA learning 12'h1: 12'hFFE: 1 to 4094 address table 12'hFFF: SA Learning without limitation
7:6	REVO	Reserved
5	SA_CNT_EN	SA Counter Enable Enable the learned source MAC Address counter. 0: Disable 1: Enable
4	SA_DIS	SA Disable Disable source MAC address learning. 0: Enable 1: Disable
3:2	SA_LOCK	SA Lock Select [NOTE] PAE frames should be passed and are not affected by SA Lock. 2'b00: Receive without SA authorization. 2'b01: All received frame whose SA look-up is missing or are not port members in the ARL will be dropped. 2'b10: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded to some Port Matrix Members (PCR.PORT_MATRIX). 2'b11: All received frames whose SA look-up is missing or are not port members in the ARL are forwarded among the Guest VLAN Member. (VTC.GUEST_MEM)
1	TX_PORT_LOCK	Tx Port Lock Enable [NOTE] PAE Frames should be passed and are not affected by Port Lock. 0: Transmit authorized. 1: Disable frame transmission.
0	RX_PORT_LOCK	Rx Port Lock Enable [NOTE] PAE frames should be passed and are not affected by Port Lock. 0: Receive authorized. 1: Disable frame receiving.

00002610				P6_PVC		Port VLAN Control of P6										810000C0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	STAG_VPID																		
Type	RW																		
Reset	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	DIS_PV_ID	FORCE_PVID	BC_LKY_V_EN	REVO	PT_OP_TION	EG_TAG			VLAN_ATTR		PORT_STAG	IPM_LK_YV_EN	MC_LK_YV_EN	UC_LKY_V_EN	ACC_FRM				
Type	RW	RW	RW	RW	RW	RW			RW		RW	RW	RW	RW	RW				
Reset	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0			

Bit(s)	Name	Description
31:16	STAG_VPID	Stack Tag VPID (VLAN Protocol ID) Value

Bit(s)	Name	Description
		The received frame will be regarded as a legal stack tag frame if the following conditions are matched: Outer VPID == STAG_VPID Inner VPID == 16'h8100 The outgoing frame will be added by the outer VLAN tag with the programmable VPID field = STAG_VPID.
15	DIS_PVID	PVID Disable Disable PVID insertion in priority-tagged frames. 0: Use PVID for priority-tagged frames. 1: Keep VID=0 for priority-tagged frames.
14	FORCE_PVID	Force PVID on VLAN-tagged frames 0: Use VID in VLAN-tagged frame. 1: Force the replacement of VID with PVID.
13	BC_LKYV_EN	Broadcast Leaky VLAN Enable 0: Broadcast frames received by this port will be blocked by VLAN. 1: Broadcast frames received by this port can pass through VLAN.
12	REVO	Reserved
11	PT_OPTION	Pass-through capability on TX special tag 0: Disable pass-through on TX special tag 1: Enable pass-through on TX special tag
10:8	EG_TAG	Incoming Port Egress VLAN Tag Attribution 3'b000: System default (disabled) 3'b001: Consistent 3'b010, 3'b011: Reserved 3'b100: Untagged 3'b101: Swap 3'b110: Tagged 3'b111: Stack
7:6	VLAN_ATTR	VLAN Port Attribute 2'b00: User port 2'b01: Stack port 2'b10: Translation port 2'b11: Transparent port
5	PORT_STAG	Special Tag Enable Enable a proprietary VLAN tag format to carry additional information to the remote port. 0: No special tag format for Tx/Rx 1: Enable
4	IPM_LKYV_EN	IP Multicast Leaky VLAN Enable (note*) If MC_LKYV_EN is set, this field will become "don't care" bit. All multicast frames including IP_Multi will be leaky between VLAN groups. 0: IP_Multi frames received by this port will be blocked by VLAN. 1: IP_Multi frames received by this port can pass through VLAN.
3	MC_LKYV_EN	Multicast Leaky VLAN Enable 0: Multicast frames received by this port will be blocked by VLAN. 1: Multicast frames received by this port can pass through VLAN.
2	UC_LKYV_EN	Unicast Leaky VLAN Enable 0: Unicast frame received by this port will be blocked by VLAN. 1: Unicast frame received by this port can pass through VLAN.
1:0	ACC_FRM	Acceptable Frame Type 2'b00: Admit All frames 2'b01: Admit Only VLAN-tagged frames 2'b10: Admit only untagged or priority-tagged frames.

Bit(s)	Name	Description
		2'b11: Reserved

00002614 P6_PPBV1 Port-and-Protocol Based VLAN I of P6 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	G1_PORT_PRI			REV0	G1_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G0_PORT_PRI			REV1	G0_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:29	G1_PORT_PRI	Group 1 Port Priority (optional) The Group 1 Priority for each port according to IEEE 802.1Q definition
28	REV0	Reserved
27:16	G1_PORT_VID	Group 1 Port VLAN ID (optional) The Group 1 VID for each port according to IEEE 802.1Q definition
15:13	G0_PORT_PRI	Group 0 Port Priority (Default Port Priority) The Group 0 and default Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G0_PORT_VID	Group 0 Port VLAN ID (Default Port VID) The Group 0 and default VID for each port according to IEEE 802.1Q definition

00002618 P6_PPBV2 Port-and-Protocol Based VLAN II of P6 00010001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name				REV0	G3_PORT_VID											
Type				RW	RW											
Reset				0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	G2_PORT_PRI			REV1	G2_PORT_VID											
Type	RW			RW	RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
28	REV0	Reserved
27:16	G3_PORT_VID	Group 3 Port VLAN ID (optional) The Group 3 VID for each port according to IEEE 802.1Q definition
15:13	G2_PORT_PRI	Group 2 Port Priority (optional) The Group 2 Priority for each port according to IEEE 802.1Q definition
12	REV1	Reserved
11:0	G2_PORT_VID	Group 2 Port VLAN ID (optional) The Group 2 VID for each port according to IEEE 802.1Q definition

0000261C P6_BSR Broadcast Storm Rate Control of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
15:8	STORM_100M	100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002620 P6_STAG01 STAG Index 0/1 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	REV0								VID1							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID1				VID0											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID1	VLAN Identifier for STAG index 1
11:0	VID0	VLAN Identifier for STAG index 0

00002624 P6_STAG23 STAG Index 2/3 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID3							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID3				VID2											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID3	VLAN Identifier for STAG index 3
11:0	VID2	VLAN Identifier for STAG index 2

00002628 P6_STAG45 STAG Index 4/5 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0								VID5							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID5				VID4											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID5	VLAN Identifier for STAG index 5
11:0	VID4	VLAN Identifier for STAG index 4

0000262C P6_STAG67 STAG Index 6/7 of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	REV0								VID7							
Type	RO								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	VID7				VID6											
Type	RW				RW											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	REV0	Reserved
23:12	VID7	VLAN Identifier for STAG index 7
11:0	VID6	VLAN Identifier for STAG index 6

00002630 P6_BSR_EXT1 Broadcast Storm Rate Control I of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control

Bit(s)	Name	Description
15:8	STORM_100M	The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps 100 Mbps Broadcast Storm Rate Limit Control
7:0	STORM_10M	The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps 10 Mbps Broadcast Storm Rate Limit Control
		The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002634 P6_BSR_EXT2 Broadcast Storm Rate Control II of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed

Bit(s)	Name	Description
15:8	STORM_100M	8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps 100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed
7:0	STORM_10M	8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps 10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed
		8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002638 P6_BSR_EXT3 Broadcast Storm Rate Control III of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STRM_MODE	STRM_BC_INC	STRM_MC_INC	STRM_UC_INC	STRM_DROP	STRM_PERD	STRM_UNIT		STORM_1G							
Type	RW	RW	RW	RW	RW	RW	RW		RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_100M								STORM_10M							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	STRM_MODE	Broadcast Storm Suppression 0: Packet-based (1 second period) 1: Rate-based
30	STRM_BC_INC	Broadcast Storm Included 0: Exclude BC frame 1: Include BC frame
29	STRM_MC_INC	Unknown Multicast Storm Included 0: Exclude MC frame 1: Include MC frame
28	STRM_UC_INC	Unknown Unicast Storm Included 0: Exclude UC frame 1: Include UC frame
27	STRM_DROP	Broadcast Storm Suppression enabled 0: BC Storm detection only 1: Enable packet drop when BC storm is detected
26	STRM_PERD	Broadcast Storm Detection Signal Period 0: One second 1: 125us
25:24	STRM_UNIT	Broadcast Storm Suppression 2'b00: 64 packets or 64 Kbps 2'b01: 256 packets or 256 Kbps 2'b10: 1 K packets or 1 Mbps 2'b11: 4 K packets or 4 Mbps
23:16	STORM_1G	1000 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 1000 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps

Bit(s)	Name	Description
15:8	STORM_100M	8'h1: (1* STORM_UNIT) packets or bps 100 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 100 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_10M	10 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 10 Mbps link speed 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002640 P6_UPW User Priority Weight of P6 00234567

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									REV0	ARL_UPW			REV1	PORT_UPW		
Type									RW	RW			RW	RW		
Reset									0	0	1	0	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV2	DSCP_UPW			REV3	TAG_UPW			REV4	STAG_UPW			REV5	ACL_UPW		
Type	RW	RW			RW	RW			RW	RW			RW	RW		
Reset	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1

Bit(s)	Name	Description
23	REV0	Reserved
22:20	ARL_UPW	ARL User Priority Weight (MAC/DIP Hit)
19	REV1	Reserved
18:16	PORT_UPW	Port-Based User Priority Weight Value Weights range from 0x0 to 0x7.
15	REV2	Reserved
14:12	DSCP_UPW	DSCP Priority Weight (IPv4)
11	REV3	Reserved
10:8	TAG_UPW	Priority Tag User Priority Weight
7	REV4	Reserved
6:4	STAG_UPW	Special Tag User Priority Weight
3	REV5	Reserved
2:0	ACL_UPW	ACL User Priority Weight (ACL Hit)

00002644 P6_PEM1 User Priority Egress Mapping I of P6 10080480

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_1			QUE_PFCR_1			QUE_PFCT_1			DSCP_PRI_1					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	1	0	0	0	0	0	0	0	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_0			QUE_PFCR_0			QUE_PFCT_0			DSCP_PRI_0					
Type	RW	RW			RW			RW			RW					
Reset	0	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_1	User Priority 1 Priority Tag Value

Bit(s)	Name	Description
27:25	QUE_PFCR_1	User Priority 1 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_1	User Priority 1 PFC TX Mapping
21:16	DSCP_PRI_1	User Priority 1 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_0	User Priority 0 Priority Tag Value
11:9	QUE_PFCR_0	User Priority 0 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_0	User Priority 0 PFC TX Mapping
5:0	DSCP_PRI_0	User Priority 0 DSCP Value

00002648 P6_PEM2 User Priority Egress Mapping II of P6 36D82250

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_3			QUE_PFCR_3			QUE_PFCT_3			DSCP_PRI_3					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_2			QUE_PFCR_2			QUE_PFCT_2			DSCP_PRI_2					
Type	RW	RW			RW			RW			RW					
Reset	0	0	1	0	0	0	1	0	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_3	User Priority 3 Priority Tag Value
27:25	QUE_PFCR_3	User Priority 3 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_3	User Priority 3 PFC TX Mapping
21:16	DSCP_PRI_3	User Priority 3 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_2	User Priority 2 Priority Tag Value
11:9	QUE_PFCR_2	User Priority 2 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_2	User Priority 2 PFC TX Mapping
5:0	DSCP_PRI_2	User Priority 2 DSCP Value

0000264C P6_PEM3 User Priority Egress Mapping III of P6 5B684920

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_5			QUE_PFCR_5			QUE_PFCT_5			DSCP_PRI_5					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	1	1	0	1	1	0	1	1	0	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_4			QUE_PFCR_4			QUE_PFCT_4			DSCP_PRI_4					
Type	RW	RW			RW			RW			RW					
Reset	0	1	0	0	1	0	0	1	0	0	1	0	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_5	User Priority 5 Priority Tag Value
27:25	QUE_PFCR_5	User Priority 5 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_5	User Priority 5 PFC TX Mapping
21:16	DSCP_PRI_5	User Priority 5 DSCP Value
15	REV1	Reserved

Bit(s)	Name	Description
14:12	TAG_PRI_4	User Priority 4 Priority Tag Value
11:9	QUE_PFCR_4	User Priority 4 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_4	User Priority 4 PFC TX Mapping
5:0	DSCP_PRI_4	User Priority 4 DSCP Value

00002650 P6_PEM4 User Priority Egress Mapping IV of P6 7FF86DB0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REV0	TAG_PRI_7			QUE_PFCR_7			QUE_PFCT_7			DSCP_PRI_7					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REV1	TAG_PRI_6			QUE_PFCR_6			QUE_PFCT_6			DSCP_PRI_6					
Type	RW	RW			RW			RW			RW					
Reset	0	1	1	0	1	1	0	1	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	REV0	Reserved
30:28	TAG_PRI_7	User Priority 7 Priority Tag Value
27:25	QUE_PFCR_7	User Priority 7 Egress Queue Selection or PFC RX Mapping
24:22	QUE_PFCT_7	User Priority 7 PFC TX Mapping
21:16	DSCP_PRI_7	User Priority 7 DSCP Value
15	REV1	Reserved
14:12	TAG_PRI_6	User Priority 6 Priority Tag Value
11:9	QUE_PFCR_6	User Priority 6 Egress Queue Selection or PFC RX Mapping
8:6	QUE_PFCT_6	User Priority 6 PFC TX Mapping
5:0	DSCP_PRI_6	User Priority 6 DSCP Value

00002654 P6_BSR_EXT4 Broadcast Storm Rate Control IV of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	STORM_2P5G_EXT3								STORM_2P5G_EXT2							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	STORM_2P5G_EXT1								STORM_2P5G							
Type	RW								RW							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	STORM_2P5G_EXT3	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
23:16	STORM_2P5G_EXT2	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

Bit(s)	Name	Description
15:8	STORM_2P5G_EXT1	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps
7:0	STORM_2P5G	2500 Mbps Broadcast Storm Rate Limit Control The broadcast storm rate limit for 2500 Mbps link speed Limitation: Max. rate limit is 1000 Mbps 8'h0: (0* STORM_UNIT) packets or bps 8'h1: (1* STORM_UNIT) packets or bps

00002658 P6_BSR_EXT5 Broadcast Storm Rate Control V of P6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	REVO															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	REVO												STRM_UNIT_1_EXT3	STRM_UNIT_1_EXT2	STRM_UNIT_1_EXT1	STRM_UNIT_1
Type	RW												RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:4	REVO	Reserved
3	STRM_UNIT_1_EXT3	Broadcast Storm Suppression 1'b1: 16 K packets or 16 Mbps
2	STRM_UNIT_1_EXT2	Broadcast Storm Suppression 1'b1: 16 K packets or 16 Mbps
1	STRM_UNIT_1_EXT1	Broadcast Storm Suppression 1'b1: 16 K packets or 16 Mbps
0	STRM_UNIT_1	Broadcast Storm Suppression 1'b1: 16 K packets or 16 Mbps

3 Scheduler (SCH)

3.1 Introduction

Since there are eight egress queues for each egress port in MT7531, a scheduler should be used to select a frame to be transmitted. In this design, three schedulers are implemented, which are Strict Priority (SP), Weight Fair Queue (WFQ), and Round-Robin (RR). However, these schedulers should co-work with the per-port maximum and minimum shapers. These functions are the main parts of the SCH (scheduler) module. Besides, the egress rate control is also implemented in this module, which supports both the leaky and token bucket algorithms.

3.2 Features

- Per queue MAX-MIN shapers with different schedulers – Strict Priority (SP), Weight Fair Queue (WFQ), Round-Robin (RR) and mixed ones
 - The minimum shapers can use either SP or RR
 - The maximum shapers can use either SP or WRQ
- Per shaper is enabled/disabled
- Per shaper threshold setting
- Per shaper with both the leaky bucket and token bucket algorithms
- Per port egress rate control with both the leaky bucket and token bucket approaches

3.3 Block Diagram

The following figure shows the functional blocks of per-port schedulers. This SCH module contains seven per-port schedules since it is a seven-port switch.

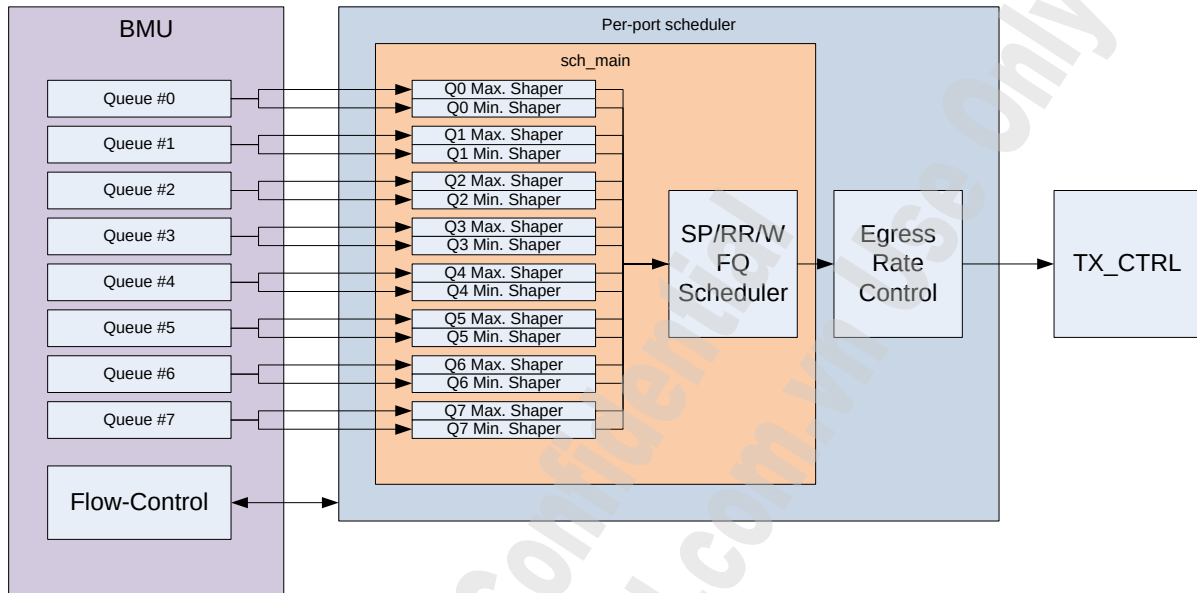


Figure 3-1 Scheduler Block Diagram

3.4 Maximum and Minimum Shapers

The following figures show the usages of minimum and maximum shapers. Both shapers can be enabled or disabled, and their thresholds can be set by registers.

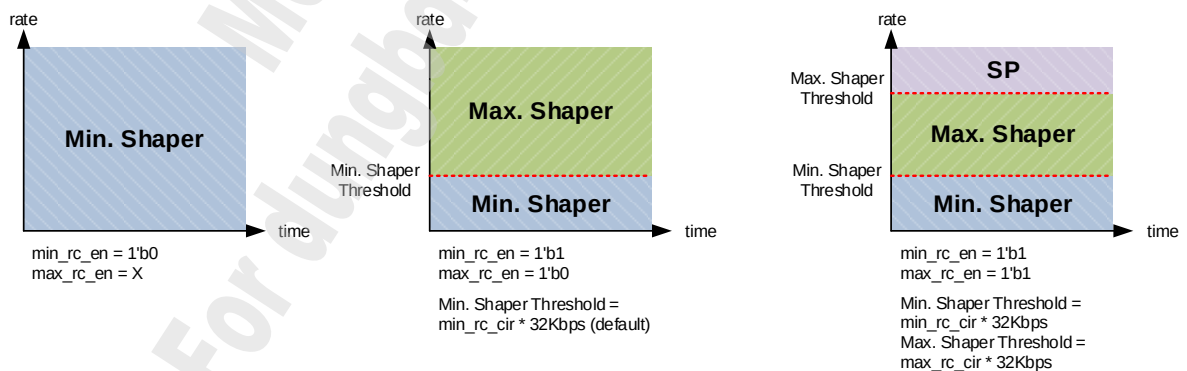


Figure 3-2 Usages of Maximum and Minimum Shapers

3.5 Register Definition

3.5.1 SCH Register

Module name: SCH Base address: (+0x0000)

Address	Name	Width	Register Function
00001000	<u>MMSCR0_Q0P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 0
00001004	<u>MMSCR1_Q0P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 0
00001008	<u>MMSCR0_Q1P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 0
0000100C	<u>MMSCR1_Q1P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 0
00001010	<u>MMSCR0_Q2P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 0
00001014	<u>MMSCR1_Q2P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 0
00001018	<u>MMSCR0_Q3P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 0
0000101C	<u>MMSCR1_Q3P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 0
00001020	<u>MMSCR0_Q4P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 0
00001024	<u>MMSCR1_Q4P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 0
00001028	<u>MMSCR0_Q5P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 0
0000102C	<u>MMSCR1_Q5P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 0
00001030	<u>MMSCR0_Q6P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 0
00001034	<u>MMSCR1_Q6P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 0
00001038	<u>MMSCR0_Q7P0</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 0
0000103C	<u>MMSCR1_Q7P0</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 0
00001040	<u>ERLCR_P0</u>	32	Egress Rate Limit Control Register of Port 0
00001050	<u>MMSCR2_Q0P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 0
00001054	<u>MMSCR3_Q0P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 0
00001058	<u>MMSCR2_Q1P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 0
0000105C	<u>MMSCR3_Q1P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 0
00001060	<u>MMSCR2_Q2P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 0
00001064	<u>MMSCR3_Q2P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 0

00001068	<u>MMSCR2_Q3P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 0
0000106C	<u>MMSCR3_Q3P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 0
00001070	<u>MMSCR2_Q4P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 0
00001074	<u>MMSCR3_Q4P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 0
00001078	<u>MMSCR2_Q5P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 0
0000107C	<u>MMSCR3_Q5P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 0
00001080	<u>MMSCR2_Q6P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 0
00001084	<u>MMSCR3_Q6P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 0
00001088	<u>MMSCR2_Q7P0</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 0
0000108C	<u>MMSCR3_Q7P0</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 0
00001090	<u>MMSCR_P0</u>	32	Max-Min Scheduler Control Register of Port 0
000010E0	<u>GERLCR</u>	32	Global Egress Rate Limit Control Register
00001100	<u>MMSCR0_Q0P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 1
00001104	<u>MMSCR1_Q0P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 1
00001108	<u>MMSCR0_Q1P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 1
0000110C	<u>MMSCR1_Q1P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 1
00001110	<u>MMSCR0_Q2P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 1
00001114	<u>MMSCR1_Q2P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 1
00001118	<u>MMSCR0_Q3P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 1
0000111C	<u>MMSCR1_Q3P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 1
00001120	<u>MMSCR0_Q4P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 1
00001124	<u>MMSCR1_Q4P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 1
00001128	<u>MMSCR0_Q5P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 1
0000112C	<u>MMSCR1_Q5P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 1
00001130	<u>MMSCR0_Q6P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 1
00001134	<u>MMSCR1_Q6P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 1
00001138	<u>MMSCR0_Q7P1</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 1

0000113C	<u>MMSCR1_Q7P1</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 1
00001140	<u>ERLCR_P1</u>	32	Egress Rate Limit Control Register of Port 1
00001150	<u>MMSCR2_Q0P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 1
00001154	<u>MMSCR3_Q0P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 1
00001158	<u>MMSCR2_Q1P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 1
0000115C	<u>MMSCR3_Q1P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 1
00001160	<u>MMSCR2_Q2P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 1
00001164	<u>MMSCR3_Q2P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 1
00001168	<u>MMSCR2_Q3P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 1
0000116C	<u>MMSCR3_Q3P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 1
00001170	<u>MMSCR2_Q4P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 1
00001174	<u>MMSCR3_Q4P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 1
00001178	<u>MMSCR2_Q5P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 1
0000117C	<u>MMSCR3_Q5P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 1
00001180	<u>MMSCR2_Q6P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 1
00001184	<u>MMSCR3_Q6P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 1
00001188	<u>MMSCR2_Q7P1</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 1
0000118C	<u>MMSCR3_Q7P1</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 1
00001190	<u>MMSCR_P1</u>	32	Max-Min Scheduler Control Register of Port 1
00001200	<u>MMSCR0_Q0P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 2
00001204	<u>MMSCR1_Q0P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 2
00001208	<u>MMSCR0_Q1P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 2
0000120C	<u>MMSCR1_Q1P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 2
00001210	<u>MMSCR0_Q2P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 2
00001214	<u>MMSCR1_Q2P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 2
00001218	<u>MMSCR0_Q3P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 2
0000121C	<u>MMSCR1_Q3P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 2

00001220	<u>MMSCR0_Q4P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 2
00001224	<u>MMSCR1_Q4P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 2
00001228	<u>MMSCR0_Q5P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 2
0000122C	<u>MMSCR1_Q5P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 2
00001230	<u>MMSCR0_Q6P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 2
00001234	<u>MMSCR1_Q6P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 2
00001238	<u>MMSCR0_Q7P2</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 2
0000123C	<u>MMSCR1_Q7P2</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 2
00001240	<u>ERLCR_P2</u>	32	Egress Rate Limit Control Register of Port 2
00001250	<u>MMSCR2_Q0P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 2
00001254	<u>MMSCR3_Q0P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 2
00001258	<u>MMSCR2_Q1P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 2
0000125C	<u>MMSCR3_Q1P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 2
00001260	<u>MMSCR2_Q2P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 2
00001264	<u>MMSCR3_Q2P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 2
00001268	<u>MMSCR2_Q3P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 2
0000126C	<u>MMSCR3_Q3P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 2
00001270	<u>MMSCR2_Q4P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 2
00001274	<u>MMSCR3_Q4P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 2
00001278	<u>MMSCR2_Q5P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 2
0000127C	<u>MMSCR3_Q5P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 2
00001280	<u>MMSCR2_Q6P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 2
00001284	<u>MMSCR3_Q6P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 2
00001288	<u>MMSCR2_Q7P2</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 2
0000128C	<u>MMSCR3_Q7P2</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 2
00001290	<u>MMSCR_P2</u>	32	Max-Min Scheduler Control Register of Port 2
00001300	<u>MMSCR0_Q0P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 3

00001304	<u>MMSCR1_Q0P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 3
00001308	<u>MMSCR0_Q1P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 3
0000130C	<u>MMSCR1_Q1P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 3
00001310	<u>MMSCR0_Q2P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 3
00001314	<u>MMSCR1_Q2P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 3
00001318	<u>MMSCR0_Q3P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 3
0000131C	<u>MMSCR1_Q3P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 3
00001320	<u>MMSCR0_Q4P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 3
00001324	<u>MMSCR1_Q4P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 3
00001328	<u>MMSCR0_Q5P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 3
0000132C	<u>MMSCR1_Q5P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 3
00001330	<u>MMSCR0_Q6P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 3
00001334	<u>MMSCR1_Q6P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 3
00001338	<u>MMSCR0_Q7P3</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 3
0000133C	<u>MMSCR1_Q7P3</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 3
00001340	<u>ERLCR_P3</u>	32	Egress Rate Limit Control Register of Port 3
00001350	<u>MMSCR2_Q0P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 3
00001354	<u>MMSCR3_Q0P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 3
00001358	<u>MMSCR2_Q1P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 3
0000135C	<u>MMSCR3_Q1P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 3
00001360	<u>MMSCR2_Q2P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 3
00001364	<u>MMSCR3_Q2P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 3
00001368	<u>MMSCR2_Q3P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 3
0000136C	<u>MMSCR3_Q3P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 3
00001370	<u>MMSCR2_Q4P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 3
00001374	<u>MMSCR3_Q4P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 3

00001378	<u>MMSCR2_Q5P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 3
0000137C	<u>MMSCR3_Q5P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 3
00001380	<u>MMSCR2_Q6P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 3
00001384	<u>MMSCR3_Q6P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 3
00001388	<u>MMSCR2_Q7P3</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 3
0000138C	<u>MMSCR3_Q7P3</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 3
00001390	<u>MMSCR_P3</u>	32	Max-Min Scheduler Control Register of Port 3
00001400	<u>MMSCR0_Q0P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 4
00001404	<u>MMSCR1_Q0P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 4
00001408	<u>MMSCR0_Q1P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 4
0000140C	<u>MMSCR1_Q1P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 4
00001410	<u>MMSCR0_Q2P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 4
00001414	<u>MMSCR1_Q2P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 4
00001418	<u>MMSCR0_Q3P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 4
0000141C	<u>MMSCR1_Q3P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 4
00001420	<u>MMSCR0_Q4P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 4
00001424	<u>MMSCR1_Q4P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 4
00001428	<u>MMSCR0_Q5P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 4
0000142C	<u>MMSCR1_Q5P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 4
00001430	<u>MMSCR0_Q6P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 4
00001434	<u>MMSCR1_Q6P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 4
00001438	<u>MMSCR0_Q7P4</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 4
0000143C	<u>MMSCR1_Q7P4</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 4
00001440	<u>ERLCR_P4</u>	32	Egress Rate Limit Control Register of Port 4
00001450	<u>MMSCR2_Q0P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 4
00001454	<u>MMSCR3_Q0P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 4
00001458	<u>MMSCR2_Q1P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 4

0000145C	<u>MMSCR3_Q1P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 4
00001460	<u>MMSCR2_Q2P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 4
00001464	<u>MMSCR3_Q2P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 4
00001468	<u>MMSCR2_Q3P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 4
0000146C	<u>MMSCR3_Q3P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 4
00001470	<u>MMSCR2_Q4P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 4
00001474	<u>MMSCR3_Q4P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 4
00001478	<u>MMSCR2_Q5P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 4
0000147C	<u>MMSCR3_Q5P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 4
00001480	<u>MMSCR2_Q6P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 4
00001484	<u>MMSCR3_Q6P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 4
00001488	<u>MMSCR2_Q7P4</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 4
0000148C	<u>MMSCR3_Q7P4</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 4
00001490	<u>MMSCR_P4</u>	32	Max-Min Scheduler Control Register of Port 4
00001500	<u>MMSCR0_Q0P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 5
00001504	<u>MMSCR1_Q0P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 5
00001508	<u>MMSCR0_Q1P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 5
0000150C	<u>MMSCR1_Q1P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 5
00001510	<u>MMSCR0_Q2P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 5
00001514	<u>MMSCR1_Q2P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 5
00001518	<u>MMSCR0_Q3P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 5
0000151C	<u>MMSCR1_Q3P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 5
00001520	<u>MMSCR0_Q4P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 5
00001524	<u>MMSCR1_Q4P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 5
00001528	<u>MMSCR0_Q5P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 5
0000152C	<u>MMSCR1_Q5P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 5

00001530	<u>MMSCR0_Q6P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 5
00001534	<u>MMSCR1_Q6P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 5
00001538	<u>MMSCR0_Q7P5</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 5
0000153C	<u>MMSCR1_Q7P5</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 5
00001540	<u>ERLCR_P5</u>	32	Egress Rate Limit Control Register of Port 5
00001550	<u>MMSCR2_Q0P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 5
00001554	<u>MMSCR3_Q0P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 5
00001558	<u>MMSCR2_Q1P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 5
0000155C	<u>MMSCR3_Q1P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 5
00001560	<u>MMSCR2_Q2P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 5
00001564	<u>MMSCR3_Q2P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 5
00001568	<u>MMSCR2_Q3P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 5
0000156C	<u>MMSCR3_Q3P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 5
00001570	<u>MMSCR2_Q4P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 5
00001574	<u>MMSCR3_Q4P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 5
00001578	<u>MMSCR2_Q5P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 5
0000157C	<u>MMSCR3_Q5P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 5
00001580	<u>MMSCR2_Q6P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 5
00001584	<u>MMSCR3_Q6P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 5
00001588	<u>MMSCR2_Q7P5</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 5
0000158C	<u>MMSCR3_Q7P5</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 5
00001590	<u>MMSCR_P5</u>	32	Max-Min Scheduler Control Register of Port 5
00001600	<u>MMSCR0_Q0P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 0/Port 6
00001604	<u>MMSCR1_Q0P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 0/Port 6
00001608	<u>MMSCR0_Q1P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 1/Port 6
0000160C	<u>MMSCR1_Q1P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 1/Port 6
00001610	<u>MMSCR0_Q2P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 2/Port 6

00001614	<u>MMSCR1_Q2P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 2/Port 6
00001618	<u>MMSCR0_Q3P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 3/Port 6
0000161C	<u>MMSCR1_Q3P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 3/Port 6
00001620	<u>MMSCR0_Q4P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 4/Port 6
00001624	<u>MMSCR1_Q4P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 4/Port 6
00001628	<u>MMSCR0_Q5P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 5/Port 6
0000162C	<u>MMSCR1_Q5P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 5/Port 6
00001630	<u>MMSCR0_Q6P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 6/Port 6
00001634	<u>MMSCR1_Q6P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 6/Port 6
00001638	<u>MMSCR0_Q7P6</u>	32	Max-Min Scheduler Control Register 0 of Queue 7/Port 6
0000163C	<u>MMSCR1_Q7P6</u>	32	Max-Min Scheduler Control Register 1 of Queue 7/Port 6
00001640	<u>ERLCR_P6</u>	32	Egress Rate Limit Control Register of Port 6
00001650	<u>MMSCR2_Q0P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 0/Port 6
00001654	<u>MMSCR3_Q0P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 0/Port 6
00001658	<u>MMSCR2_Q1P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 1/Port 6
0000165C	<u>MMSCR3_Q1P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 1/Port 6
00001660	<u>MMSCR2_Q2P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 2/Port 6
00001664	<u>MMSCR3_Q2P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 2/Port 6
00001668	<u>MMSCR2_Q3P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 3/Port 6
0000166C	<u>MMSCR3_Q3P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 3/Port 6
00001670	<u>MMSCR2_Q4P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 4/Port 6
00001674	<u>MMSCR3_Q4P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 4/Port 6
00001678	<u>MMSCR2_Q5P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 5/Port 6
0000167C	<u>MMSCR3_Q5P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 5/Port 6
00001680	<u>MMSCR2_Q6P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 6/Port 6
00001684	<u>MMSCR3_Q6P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 6/Port 6

00001688	<u>MMSCR2_Q7P6</u>	32	Max-Min Scheduler Control Register 2 of Queue 7/Port 6
0000168C	<u>MMSCR3_Q7P6</u>	32	Max-Min Scheduler Control Register 3 of Queue 7/Port 6
00001690	<u>MMSCR_P6</u>	32	Max-Min Scheduler Control Register of Port 6

00001000 MMSCRO_Q0P0

Max-Min Scheduler Control Register 0 of Queue 0/Port 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P0				MIN_RATE_CTRL_EXP_TB_T_Q0_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P0	Port 0 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P0	Port 0 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 0 min. shaper rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms

Bit(s)	Name	Description
		9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 0 min. shaper rate limit control, value range: 1..255 In MT7531AE/BE, Final Rate Limit = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Final Rate Limit = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping, and Token Bucket = $Max (MIN\_RATE\_CIR * TB\_T, TB\_CBS * 512)$

00001004 MMSCR1_Q0P0 Max-Min Scheduler Control Register 1 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P0				MAX_WEIGHT_Q0_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P0				MAX_RATE_CTRL_EXP_TB_T_Q0_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P0	Port 0 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P0	Port 0 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P0	Port 0 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 0 max. shaper rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps

Bit(s)	Name	Description
		5: 100Mbps When MIN_MAX_TB_EN = 1, TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 0 max. shaper rate limit control, value range: 1..255 In MT7531AE/BE, Final Rate Limit = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Final Rate Limit = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping, and Token Bucket = $Max (MAX\_RATE\_CIR * TB\_T, TB\_CBS * 512)$

00001008 **MMSCRO_Q1P0** Max-Min Scheduler Control Register 0 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P0				MIN_RATE_CTRL_EXP_TB_T_Q1_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P0	Port 0 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P0	Port 0 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P0	1: Queue 1 min. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 1 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000100C MMSCR1_Q1P0 Max-Min Scheduler Control Register 1 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P0				MAX_WEIGHT_Q1_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P0				MAX_RATE_CTRL_EXP_TB_T_Q1_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P0	Port 0 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P0	Port 0 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P0	Port 0 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 1 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 1 max. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001010 **MMSCRO_Q2P0** Max-Min Scheduler Control Register 0 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P0				MIN_RATE_CTRL_EXP_TB_T_Q2_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P0	Port 0 Queue 2 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P0	Port 0 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 2 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001014 **MMSCR1_Q2P0** Max-Min Scheduler Control Register 1 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P0				MAX_WEIGHT_Q2_P0											
Type	RW				RW											

Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P0				MAX_RATE_CTRL_EXP_TB_T_Q2_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P0	Port 0 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P0	Port 0 Queue 2 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P0	Port 0 Queue 2 max. shaper rate limit control is enabled 0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001018 MMSCRO_Q3P0 Max-Min Scheduler Control Register 0 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P0				MIN_RATE_CTRL_EXP_TB_T_Q3_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P0	Port 0 Queue 3 min. traffic arbitration scheme

Bit(s)	Name	Description
		0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P0	Port 0 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 3 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000101C MMSCR1_Q3P0

Max-Min Scheduler Control Register 1 of Queue 3/Port 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P0				MAX_WEIGHT_Q3_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P0				MAX_RATE_CTRL_EXP_TB_T_Q3_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P0	Port 0 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P0	Port 0 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P0	Port 0 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001020 **MMSCRO_Q4P0** Max-Min Scheduler Control Register 0 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P0				MIN_RATE_CTRL_EXP_TB_T_Q4_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P0	Port 0 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P0	Port 0 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001024 **MMSCR1_Q4P0** Max-Min Scheduler Control Register 1 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MAX_SP_WFQ_Q4_P0				MAX_WEIGHT_Q4_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P0				MAX_RATE_CTRL_EXP_TB_T_Q4_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q4_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P0	Port 0 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P0	Port 0 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P0	Port 0 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001028 **MMSCRO_Q5P0** Max-Min Scheduler Control Register 0 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P0				MIN_RATE_CTRL_EXP_TB_T_Q5_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q5_P0							
Type	RW				RW				RW							

Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P0	Port 0 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P0	Port 0 Queue 5 min. shaper rate limit control is enabled 0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 5 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000102C MMSCR1_Q5P0

Max-Min Scheduler Control Register 1 of Queue 5/Port 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P0				MAX_WEIGHT_Q5_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P0				MAX_RATE_CTRL_EXP_TB_T_Q5_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q5_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P0	Port 0 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P0	Port 0 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P0	Port 0 Queue 5 max. shaper rate limit control is enabled 0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P0	When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 5 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001030 **MMSCRO_Q6P0** Max-Min Scheduler Control Register 0 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P0				MIN_RATE_CTRL_EXP_TB_T_Q6_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q6_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P0	Port 0 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P0	Port 0 Queue 6 min. shaper rate limit control is enabled 0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 6 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001034

MMSCR1_Q6P0

Max-Min Scheduler Control Register 1 of Queue
6/Port 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P0				MAX_WEIGHT_Q6_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P0				MAX_RATE_CTRL_EXP_TB_T_Q6_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P0	Port 0 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P0	Port 0 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P0	Port 0 Queue 6 max. shaper rate limit control is enabled 0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 6 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001038

MMSCRO_Q7P0

Max-Min Scheduler Control Register 0 of Queue
7/Port 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P0															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P0				MIN_RATE_CTRL_EXP_TB_T_Q7_P0				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P0							

	N_Q7_P0															
Type	RW															
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P0	Port 0 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P0	Port 0 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P0	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 7 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000103C MMSCR1_Q7P0

Max-Min Scheduler Control Register 1 of Queue 7/Port 0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P0				MAX_WEIGHT_Q7_P0											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P0				MAX_RATE_CTRL_EXP_TB_T_Q7_P0				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P0							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P0	Port 0 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P0	Port 0 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P0	Port 0 Queue 7 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P0	0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 0 Queue 7 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P0	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 0 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001040			ERLCR_P0		Egress Rate Limit Control Register of Port 0												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	EGC_RATE_CIR_15_0_P0																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	EG_RA TE_LIM IT_EN_ P0	EGC_T B_EN_ P0		EGC_R ATE_CI R_16_P 0	EG_RATE_LIMIT_EXP_P0_EGC_ TB_T_P0				EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0										
Type	RW	RW		RW	RW				RW										
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P0	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = [\text{Egress Port Rate Limitation}(\text{bps}) / 8 * (1/EGC\_TB\_T) (\text{bps})]$ In MT7531DE, $EGC\_RATE\_CIR = [2 * \text{Egress Port Rate Limitation}(\text{bps}) / 8 * (1/EGC\_TB\_T) (\text{bps})]$
15	EG_RATE_LIMIT_EN_P0	Port 0 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P0	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	EGC_RATE_CIR_16_P0	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	EG_RATE_LIMIT_EXP_P0_EGC_TB_T_P0	Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 0 Egress rate limit control, value range: 0..5 0: 1Kbps

Bit(s)	Name	Description
		1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	EG_RATE_LIMIT_MAN_P0_EGC_TB_CBS_P0	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When EGC_TB_EN = 0, mantissa part of Port 0 Egress rate limit control, value range: 1..255 In MT7531AE/BE, Egress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Egress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (EGC\_RATE\_CIR * EGC\_TB\_T, EGC\_TB\_CBS * 512)$

00001050 **MMSCR2_Q0P0** Max-Min Scheduler Control Register 2 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P0	When MIN_MAX_TB_EN = 1, total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $MIN\_RATE\_CIR = [MIN\ Shaper\ Rate\ Limitation / 8 * (1/TB\_T)]\ bps$

Bit(s)	Name	Description
		In MT7531DE, MIN_RATE_CIR = [2 * MIN Shaper Rate Limitation / 8 * (1/TB_T)] bps

00001054 MMSCR3_Q0P0 Max-Min Scheduler Control Register 3 of Queue 0/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P0	When MIN_MAX_TB_EN = 1, total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, MAX_RATE_CIR = [MAX Shaper Rate Limitation / 8 * (1/TB_T)] bps In MT7531DE, MAX_RATE_CIR = [2 * MAX Shaper Rate Limitation / 8 * (1/TB_T)] bps

00001058 MMSCR2_Q1P0 Max-Min Scheduler Control Register 2 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000105C MMSCR3_Q1P0 Max-Min Scheduler Control Register 3 of Queue 1/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001060 MMSCR2_Q2P0 Max-Min Scheduler Control Register 2 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q2_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001064 MMSCR3_Q2P0 Max-Min Scheduler Control Register 3 of Queue 2/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001068 **MMSCR2_Q3P0** Max-Min Scheduler Control Register 2 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000106C **MMSCR3_Q3P0** Max-Min Scheduler Control Register 3 of Queue 3/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001070 **MMSCR2_Q4P0** Max-Min Scheduler Control Register 2 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P0

																R_Q4_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001074 MMSCR3_Q4P0 Max-Min Scheduler Control Register 3 of Queue 4/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001078 MMSCR2_Q5P0 Max-Min Scheduler Control Register 2 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000107C **MMSCR3_Q5P0** Max-Min Scheduler Control Register 3 of Queue 5/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001080 **MMSCR2_Q6P0** Max-Min Scheduler Control Register 2 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001084 **MMSCR3_Q6P0** Max-Min Scheduler Control Register 3 of Queue 6/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P0

																R_Q6_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001088 MMSCR2_Q7P0 Max-Min Scheduler Control Register 2 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P0	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000108C MMSCR3_Q7P0 Max-Min Scheduler Control Register 3 of Queue 7/Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P0
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P0	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001090 MMSCR_P0 Max-Min Scheduler Control Register of Port 0 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P0
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P0	When this bit is disabled, the rate limit acts like a leaky bucket principle. Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

000010E0 GERLCR Global Egress Rate Limit Control Register 00000118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							EGC_MFRM_EX	EGC_IPG_OP	EGC_IPG_BYTE							
Type							RW	RW	RW							
Reset							0	1	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
9	EGC_MFRM_EX	When this bit is enabled, management frames are excluded in the egress rate limit control mechanism; otherwise, management frames are included. (Management frame type is set by ARL registers) 0: Include management frames 1: Exclude management frames
8	EGC_IPG_OP	Egress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted for the rate calculation. 0: IPG byte is excluded 1: IPG byte is included

Bit(s)	Name	Description
7:0	EGC_IPG_BYTE	Egress Rate IPG Byte Count Byte count should be added while calculating the rate limit. 0x04: 4 byte CRC 0x18: 4 byte CRC + 12 byte IPG + 8 byte Preamble (default)

00001100 **MMSCRO_Q0P1** Max-Min Scheduler Control Register 0 of Queue 0/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P1				MIN_RATE_CTRL_EXP_TB_T_Q0_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P1	Port 1 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P1	Port 1 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 0 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 0 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001104 **MMSCR1_Q0P1** Max-Min Scheduler Control Register 1 of Queue 0/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ				MAX_WEIGHT_Q0_P1											

	_Q0_P1															
Type	RW															
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P1				MAX_RATE_CTRL_EXP_TB_T_Q0_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P1							
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P1	Port 1 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P1	Port 1 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P1	Port 1 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 0 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 0 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001108 MMSCRO_Q1P1 Max-Min Scheduler Control Register 0 of Queue 1/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P1				MIN_RATE_CTRL_EXP_TB_T_Q1_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P1							
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P1	Port 1 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P1	Port 1 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 1 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000110C **MMSCR1_Q1P1** Max-Min Scheduler Control Register 1 of Queue 1/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P1				MAX_WEIGHT_Q1_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P1				MAX_RATE_CTRL_EXP_TB_T_Q1_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P1	Port 1 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P1	Port 1 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P1	Port 1 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 1 max. shaper rate limit control, value range: 0..5

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P1	When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 1 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001110 MMSCRO_Q2P1 Max-Min Scheduler Control Register 0 of Queue 2/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P1				MIN_RATE_CTRL_EXP_TB_T_Q2_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P1	Port 1 Queue 2 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P1	Port 1 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 2 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001114 MMSCR1_Q2P1 Max-Min Scheduler Control Register 1 of Queue 2/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P1				MAX_WEIGHT_Q2_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P1				MAX_RATE_CTRL_EXP_TB_T_Q2_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P1	Port 1 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P1	Port 1 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P1	Port 1 Queue 2 max. shaper rate limit control is enabled 0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001118 **MMSCRO_Q3P1** Max-Min Scheduler Control Register 0 of Queue 3/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P1				MIN_RATE_CTRL_EXP_TB_T_Q3_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P1							

Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P1	Port 1 Queue 3 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P1	Port 1 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 3 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000111C MMSCR1_Q3P1

Max-Min Scheduler Control Register 1 of Queue
3/Port 1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P1				MAX_WEIGHT_Q3_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P1				MAX_RATE_CTRL_EXP_TB_T_Q3_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P1	Port 1 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P1	Port 1 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P1	Port 1 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001120 **MMSCRO_Q4P1** Max-Min Scheduler Control Register 0 of Queue 4/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P1				MIN_RATE_CTRL_EXP_TB_T_Q4_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P1	Port 1 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P1	Port 1 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001124

MMSCR1_Q4P1

Max-Min Scheduler Control Register 1 of Queue
4/Port 1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P1				MAX_WEIGHT_Q4_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P1				MAX_RATE_CTRL_EXP_TB_T_Q4_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q4_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P1	Port 1 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P1	Port 1 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P1	Port 1 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001128

MMSCR0_Q5P1

Max-Min Scheduler Control Register 0 of Queue
5/Port 1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MIN_RATE_EN_Q5_P1				MIN_RATE_CTRL_EXP_TB_T_Q5_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q5_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P1	Port 1 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P1	Port 1 Queue 5 min. shaper rate limit control is enabled 0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 5 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000112C **MMSCR1_Q5P1** Max-Min Scheduler Control Register 1 of Queue 5/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P1				MAX_WEIGHT_Q5_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P1				MAX_RATE_CTRL_EXP_TB_T_Q5_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q5_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P1	Port 1 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P1	Port 1 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P1	Port 1 Queue 5 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P1	0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 5 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001130 MMSCRO_Q6P1

Max-Min Scheduler Control Register 0 of Queue 6/Port 1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P1				MIN_RATE_CTRL_EXP_TB_T_Q6_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q6_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P1	Port 1 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P1	Port 1 Queue 6 min. shaper rate limit control is enabled 0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 6 min. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001134 **MMSCR1_Q6P1** Max-Min Scheduler Control Register 1 of Queue 6/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P1				MAX_WEIGHT_Q6_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P1				MAX_RATE_CTRL_EXP_TB_T_Q6_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P1	Port 1 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P1	Port 1 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P1	Port 1 Queue 6 max. shaper rate limit control is enabled 0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 6 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001138 **MMSCR0_Q7P1** Max-Min Scheduler Control Register 0 of Queue 7/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR															

	_Q7_P1															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P1				MIN_RATE_CTRL_EXP_TB_T_Q7_P1				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P1	Port 1 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P1	Port 1 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 7 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000113C MMSCR1_Q7P1

Max-Min Scheduler Control Register 1 of Queue 7/Port 1

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P1				MAX_WEIGHT_Q7_P1											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P1				MAX_RATE_CTRL_EXP_TB_T_Q7_P1				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P1							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P1	Port 1 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P1	Port 1 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P1	Port 1 Queue 7 max. shaper rate limit control is enabled 0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P1	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 1 Queue 7 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P1	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 1 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001140		ERLCR_P1		Egress Rate Limit Control Register of Port 1												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	EGC_RATE_CIR_15_0_P1																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	EG_RA TE_LIM IT_EN_ P1	EGC_T B_EN_ P1		EGC_R ATE_CI R_16_P 1	EG_RATE_LIMIT_EXP_P1_EGC_ TB_T_P1				EG_RATE_LIMIT_MAN_P1_EGC_TB_CBS_P1								
Type	RW	RW		RW	RW				RW								
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P1	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = \lceil \text{Egress Port Rate Limitation(bps)} / 8 * (1/EGC\_TB\_T) \rceil$ (bps) In MT7531DE, $EGC\_RATE\_CIR = \lceil 2 * \text{Egress Port Rate Limitation(bps)} / 8 * (1/EGC\_TB\_T) \rceil$ (bps)
15	EG_RATE_LIMIT_EN_P1	Port 1 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P1	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

Bit(s)	Name	Description
12	EGC_RATE_CIR_16_P1	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	EG_RATE_LIMIT_EXP_P1_EGC_TB_T_P1	Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 1 Egress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	EG_RATE_LIMIT_MAN_P1_EGC_TB_CBS_P1	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When EGC_TB_EN = 0, mantissa part of Port 1 Egress rate limit control, value range: 1..255 In MT7531AE/BE, Egress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Egress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001150 MMSCR2_Q0P1 Max-Min Scheduler Control Register 2 of Queue 0/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001154 **MMSCR3_Q0P1** Max-Min Scheduler Control Register 3 of Queue 0/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001158 **MMSCR2_Q1P1** Max-Min Scheduler Control Register 2 of Queue 1/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000115C **MMSCR3_Q1P1** Max-Min Scheduler Control Register 3 of Queue 1/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P1

																R_Q1_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001160 MMSCR2_Q2P1 Max-Min Scheduler Control Register 2 of Queue 2/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q2_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001164 MMSCR3_Q2P1 Max-Min Scheduler Control Register 3 of Queue 2/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001168 **MMSCR2_Q3P1** Max-Min Scheduler Control Register 2 of Queue 3/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000116C **MMSCR3_Q3P1** Max-Min Scheduler Control Register 3 of Queue 3/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001170 **MMSCR2_Q4P1** Max-Min Scheduler Control Register 2 of Queue 4/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P1

																R_Q4_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001174 MMSCR3_Q4P1 Max-Min Scheduler Control Register 3 of Queue 4/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001178 MMSCR2_Q5P1 Max-Min Scheduler Control Register 2 of Queue 5/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000117C **MMSCR3_Q5P1** Max-Min Scheduler Control Register 3 of Queue 5/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001180 **MMSCR2_Q6P1** Max-Min Scheduler Control Register 2 of Queue 6/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001184 **MMSCR3_Q6P1** Max-Min Scheduler Control Register 3 of Queue 6/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P1

																R_Q6_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001188 MMSCR2_Q7P1 Max-Min Scheduler Control Register 2 of Queue 7/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P1	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000118C MMSCR3_Q7P1 Max-Min Scheduler Control Register 3 of Queue 7/Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P1
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P1	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001190 MMSCR_P1 Max-Min Scheduler Control Register of Port 1 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P1
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P1	When this bit is disabled, the rate limit acts like a leaky bucket principle. Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

00001200 MMSCR_Q0P2 Max-Min Scheduler Control Register 0 of Queue 0/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P2				MIN_RATE_CTRL_EXP_TB_T_Q0_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P2	Port 2 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P2	Port 2 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate)

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P2	1: Queue 0 min. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 0 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 0 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001204 MMSCR1_Q0P2 Max-Min Scheduler Control Register 1 of Queue 0/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P2				MAX_WEIGHT_Q0_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P2				MAX_RATE_CTRL_EXP_TB_T_Q0_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P2	Port 2 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P2	Port 2 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P2	Port 2 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 0 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 0 max. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001208 **MMSCRO_Q1P2** Max-Min Scheduler Control Register 0 of Queue 1/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P2				MIN_RATE_CTRL_EXP_TB_T_Q1_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P2	Port 2 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P2	Port 2 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 1 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000120C **MMSCR1_Q1P2** Max-Min Scheduler Control Register 1 of Queue 1/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P2				MAX_WEIGHT_Q1_P2											
Type	RW				RW											

Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P2				MAX_RATE_CTRL_EXP_TB_T_Q1_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P2	Port 2 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P2	Port 2 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P2	Port 2 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 1 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 1 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001210 **MMSCRO_Q2P2** Max-Min Scheduler Control Register 0 of Queue 2/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P2				MIN_RATE_CTRL_EXP_TB_T_Q2_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P2	Port 2 Queue 2 min. traffic arbitration scheme

Bit(s)	Name	Description
		0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P2	Port 2 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 2 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001214 **MMSCR1_Q2P2** Max-Min Scheduler Control Register 1 of Queue 2/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P2				MAX_WEIGHT_Q2_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P2				MAX_RATE_CTRL_EXP_TB_T_Q2_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P2	Port 2 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P2	Port 2 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P2	Port 2 Queue 2 max. shaper rate limit control is enabled 0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001218 MMSCRO_Q3P2 Max-Min Scheduler Control Register 0 of Queue 3/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P2				MIN_RATE_CTRL_EXP_TB_T_Q3_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P2	Port 2 Queue 3 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P2	Port 2 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 3 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000121C MMSCR1_Q3P2 Max-Min Scheduler Control Register 1 of Queue 3/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MAX_SP_WFQ_Q3_P2				MAX_WEIGHT_Q3_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P2				MAX_RATE_CTRL_EXP_TB_T_Q3_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P2	Port 2 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P2	Port 2 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P2	Port 2 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001220 MMSCRO_Q4P2 Max-Min Scheduler Control Register 0 of Queue 4/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P2				MIN_RATE_CTRL_EXP_TB_T_Q4_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P2							
Type	RW				RW				RW							

Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P2	Port 2 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P2	Port 2 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001224 MMSCR1_Q4P2

Max-Min Scheduler Control Register 1 of Queue
4/Port 2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P2				MAX_WEIGHT_Q4_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P2				MAX_RATE_CTRL_EXP_TB_T_Q4_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q4_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P2	Port 2 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P2	Port 2 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P2	Port 2 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P2	When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001228 MMSCRO_Q5P2 Max-Min Scheduler Control Register 0 of Queue 5/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P2				MIN_RATE_CTRL_EXP_TB_T_Q5_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q5_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P2	Port 2 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P2	Port 2 Queue 5 min. shaper rate limit control is enabled 0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 5 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000122C

MMSCR1_Q5P2

Max-Min Scheduler Control Register 1 of Queue
5/Port 2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P2				MAX_WEIGHT_Q5_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P2				MAX_RATE_CTRL_EXP_TB_T_Q5_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q5_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P2	Port 2 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P2	Port 2 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P2	Port 2 Queue 5 max. shaper rate limit control is enabled 0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 5 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001230

MMSCRO_Q6P2

Max-Min Scheduler Control Register 0 of Queue
6/Port 2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P2				MIN_RATE_CTRL_EXP_TB_T_Q6_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q6_P2							

	N_Q6_P2															
Type	RW															
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P2	Port 2 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P2	Port 2 Queue 6 min. shaper rate limit control is enabled 0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 6 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001234 **MMSCR1_Q6P2** Max-Min Scheduler Control Register 1 of Queue 6/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P2				MAX_WEIGHT_Q6_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P2				MAX_RATE_CTRL_EXP_TB_T_Q6_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P2	Port 2 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P2	Port 2 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P2	Port 2 Queue 6 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P2	0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 6 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001238 **MMSCRO_Q7P2** Max-Min Scheduler Control Register 0 of Queue 7/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P2															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P2				MIN_RATE_CTRL_EXP_TB_T_Q7_P2				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P2	Port 2 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P2	Port 2 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 7 min. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000123C **MMSCR1_Q7P2** Max-Min Scheduler Control Register 1 of Queue 7/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P2				MAX_WEIGHT_Q7_P2											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P2				MAX_RATE_CTRL_EXP_TB_T_Q7_P2				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P2							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P2	Port 2 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P2	Port 2 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P2	Port 2 Queue 7 max. shaper rate limit control is enabled 0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P2	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 2 Queue 7 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P2	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 2 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001240 **ERLCR_P2** Egress Rate Limit Control Register of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P2	EGC_TB_EN_P2		EGC_RATE_CIR_16_P2	EG_RATE_LIMIT_EXP_P2_EGC_TB_T_P2				EG_RATE_LIMIT_MAN_P2_EGC_TB_CBS_P2							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P2	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = \lceil \text{Egress Port Rate Limitation(bps)} / 8 * (1/EGC\_TB\_T) \rceil$ (bps)] In MT7531DE, $EGC\_RATE\_CIR = \lceil 2 * \text{Egress Port Rate Limitation(bps)} / 8 * (1/EGC\_TB\_T) \rceil$ (bps)]
15	EG_RATE_LIMIT_EN_P2	Port 2 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P2	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	EGC_RATE_CIR_16_P2	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	EG_RATE_LIMIT_EXP_P2_EGC_TB_T_P2	Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 2 Egress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	EG_RATE_LIMIT_MAN_P2_EGC_TB_CBS_P2	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket

Bit(s)	Name	Description
		When EGC_TB_EN = 0, mantissa part of Port 2 Egress rate limit control, value range: 1..255 In MT7531AE/BE, Egress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Egress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (EGC\_RATE\_CIR * EGC\_TB\_T, EGC\_TB\_CBS * 512)$

00001250 **MMSCR2_Q0P2** Max-Min Scheduler Control Register 2 of Queue 0/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001254 **MMSCR3_Q0P2** Max-Min Scheduler Control Register 3 of Queue 0/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001258

MMSCR2_Q1P2

Max-Min Scheduler Control Register 2 of Queue
1/Port 2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000125C

MMSCR3_Q1P2

Max-Min Scheduler Control Register 3 of Queue
1/Port 2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001260

MMSCR2_Q2P2

Max-Min Scheduler Control Register 2 of Queue
2/Port 2

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q2_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P2															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001264 MMSCR3_Q2P2 Max-Min Scheduler Control Register 3 of Queue 2/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001268 MMSCR2_Q3P2 Max-Min Scheduler Control Register 2 of Queue 3/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000126C MMSCR3_Q3P2 Max-Min Scheduler Control Register 3 of Queue 3/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001270 **MMSCR2_Q4P2** Max-Min Scheduler Control Register 2 of Queue 4/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001274 **MMSCR3_Q4P2** Max-Min Scheduler Control Register 3 of Queue 4/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001278 **MMSCR2_Q5P2** Max-Min Scheduler Control Register 2 of Queue 5/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000127C **MMSCR3_Q5P2** Max-Min Scheduler Control Register 3 of Queue 5/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001280 **MMSCR2_Q6P2** Max-Min Scheduler Control Register 2 of Queue 6/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P2

																R_Q6_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001284 MMSCR3_Q6P2 Max-Min Scheduler Control Register 3 of Queue 6/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001288 MMSCR2_Q7P2 Max-Min Scheduler Control Register 2 of Queue 7/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P2	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000128C **MMSCR3_Q7P2** Max-Min Scheduler Control Register 3 of Queue 7/Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P2
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P2	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001290 **MMSCR_P2** Max-Min Scheduler Control Register of Port 2 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P2
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P2	When this bit is disabled, the rate limit acts like a leaky bucket principle. Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

00001300 **MMSCR0_Q0P3** Max-Min Scheduler Control Register 0 of Queue 0/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	MIN_SP_WRR_Q0_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P3				MIN_RATE_CTRL_EXP_TB_T_Q0_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P3	Port 3 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P3	Port 3 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 0 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 0 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001304 MMSCR1_Q0P3 Max-Min Scheduler Control Register 1 of Queue 0/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P3				MAX_WEIGHT_Q0_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P3				MAX_RATE_CTRL_EXP_TB_T_Q0_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P3	Port 3 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P3	Port 3 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P3	Port 3 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 0 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 0 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001308 **MMSCRO_Q1P3** Max-Min Scheduler Control Register 0 of Queue 1/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P3				MIN_RATE_CTRL_EXP_TB_T_Q1_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P3	Port 3 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P3	Port 3 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 1 min. shaper rate limit control, value range: 0..5

Bit(s)	Name	Description
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P3	When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000130C MMSCR1_Q1P3 Max-Min Scheduler Control Register 1 of Queue 1/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P3				MAX_WEIGHT_Q1_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P3				MAX_RATE_CTRL_EXP_TB_T_Q1_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P3	Port 3 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P3	Port 3 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P3	Port 3 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 1 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 1 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001310

MMSCRO_Q2P3

Max-Min Scheduler Control Register 0 of Queue
2/Port 3

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P3				MIN_RATE_CTRL_EXP_TB_T_Q2_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P3	Port 3 Queue 2 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P3	Port 3 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 2 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001314

MMSCR1_Q2P3

Max-Min Scheduler Control Register 1 of Queue
2/Port 3

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P3				MAX_WEIGHT_Q2_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P3				MAX_RATE_CTRL_EXP_TB_T_Q2_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P3							

Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P3	Port 3 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P3	Port 3 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P3	Port 3 Queue 2 max. shaper rate limit control is enabled 0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001318 MMSCR0_Q3P3

Max-Min Scheduler Control Register 0 of Queue 3/Port 3

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P3				MIN_RATE_CTRL_EXP_TB_T_Q3_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P3	Port 3 Queue 3 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P3	Port 3 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 3 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000131C **MMSCR1_Q3P3** Max-Min Scheduler Control Register 1 of Queue 3/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P3				MAX_WEIGHT_Q3_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P3				MAX_RATE_CTRL_EXP_TB_T_Q3_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P3	Port 3 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P3	Port 3 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P3	Port 3 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

Bit(s)	Name	Description

00001320 MMSCRO_Q4P3 Max-Min Scheduler Control Register 0 of Queue 4/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P3				MIN_RATE_CTRL_EXP_TB_T_Q4_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P3	Port 3 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P3	Port 3 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001324 MMSCR1_Q4P3 Max-Min Scheduler Control Register 1 of Queue 4/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P3				MAX_WEIGHT_Q4_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MAX_RATE_EN_Q4_P3				MAX_RATE_CTRL_EXP_TB_T_Q4_P3					MAX_RATE_CTRL_MAN_TB_CBS_Q4_P3						
Type	RW				RW					RW						
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P3	Port 3 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P3	Port 3 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P3	Port 3 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001328 **MMSCRO_Q5P3** Max-Min Scheduler Control Register 0 of Queue 5/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P3				MIN_RATE_CTRL_EXP_TB_T_Q5_P3											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P3	Port 3 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P3	Port 3 Queue 5 min. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P3	0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 5 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000132C MMSCR1_Q5P3

Max-Min Scheduler Control Register 1 of Queue 5/Port 3

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P3				MAX_WEIGHT_Q5_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P3				MAX_RATE_CTRL_EXP_TB_T_Q5_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q5_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P3	Port 3 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P3	Port 3 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P3	Port 3 Queue 5 max. shaper rate limit control is enabled 0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 5 max. shaper rate limit control, value range: 1..255
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001330 **MMSCRO_Q6P3** Max-Min Scheduler Control Register 0 of Queue 6/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P3				MIN_RATE_CTRL_EXP_TB_T_Q6_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q6_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P3	Port 3 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P3	Port 3 Queue 6 min. shaper rate limit control is enabled 0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 6 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001334 **MMSCR1_Q6P3** Max-Min Scheduler Control Register 1 of Queue 6/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ				MAX_WEIGHT_Q6_P3											

	_Q6_P3															
Type	RW															
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P3				MAX_RATE_CTRL_EXP_TB_T_Q6_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P3							
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P3	Port 3 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P3	Port 3 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P3	Port 3 Queue 6 max. shaper rate limit control is enabled 0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 6 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001338 MMSCRO_Q7P3 Max-Min Scheduler Control Register 0 of Queue 7/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P3															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P3				MIN_RATE_CTRL_EXP_TB_T_Q7_P3				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P3							
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P3	Port 3 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P3	Port 3 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P3	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 7 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000133C **MMSCR1_Q7P3** **Max-Min Scheduler Control Register 1 of Queue 7/Port 3** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P3				MAX_WEIGHT_Q7_P3											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P3				MAX_RATE_CTRL_EXP_TB_T_Q7_P3				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P3							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P3	Port 3 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P3	Port 3 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P3	Port 3 Queue 7 max. shaper rate limit control is enabled 0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P3	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 3 Queue 7 max. shaper rate limit control, value range: 0..5

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P3	When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 3 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001340 ERLCR_P3 Egress Rate Limit Control Register of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P3	EGC_TB_EN_P3		EGC_RATE_CIR_16_P3	EG_RATE_LIMIT_EXP_P3_EGC_TB_T_P3					EG_RATE_LIMIT_MAN_P3_EGC_TB_CBS_P3						
Type	RW	RW		RW	RW					RW						
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P3	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = \lfloor \text{Egress Port Rate Limitation}(\text{bps}) / 8 * (1/EGC\_TB\_T) (\text{bps}) \rfloor$ In MT7531DE, $EGC\_RATE\_CIR = \lfloor 2 * \text{Egress Port Rate Limitation}(\text{bps}) / 8 * (1/EGC\_TB\_T) (\text{bps}) \rfloor$
15	EG_RATE_LIMIT_EN_P3	Port 3 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P3	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	EGC_RATE_CIR_16_P3	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 3 Egress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14
11:8	EG_RATE_LIMIT_EXP_P3_EGC_TB_T_P3	

Bit(s)	Name	Description
		0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	EG_RATE_LIMIT_MAN_P3_EGC_TB_CBS_P3	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When EGC_TB_EN = 0, mantissa part of Port 3 Egress rate limit control, value range: 1..255 In MT7531AE/BE, Egress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Egress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (EGC\_RATE\_CIR * EGC\_TB\_T, EGC\_TB\_CBS * 512)$

00001350 **MMSCR2_Q0P3** Max-Min Scheduler Control Register 2 of Queue 0/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001354 **MMSCR3_Q0P3** Max-Min Scheduler Control Register 3 of Queue 0/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P3

																R_Q0_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001358 MMSCR2_Q1P3 Max-Min Scheduler Control Register 2 of Queue 1/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000135C MMSCR3_Q1P3 Max-Min Scheduler Control Register 3 of Queue 1/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001360 **MMSCR2_Q2P3** Max-Min Scheduler Control Register 2 of Queue 2/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q2_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001364 **MMSCR3_Q2P3** Max-Min Scheduler Control Register 3 of Queue 2/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001368 **MMSCR2_Q3P3** Max-Min Scheduler Control Register 2 of Queue 3/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P3

																R_Q3_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000136C MMSCR3_Q3P3 Max-Min Scheduler Control Register 3 of Queue 3/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001370 MMSCR2_Q4P3 Max-Min Scheduler Control Register 2 of Queue 4/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001374 **MMSCR3_Q4P3** Max-Min Scheduler Control Register 3 of Queue 4/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001378 **MMSCR2_Q5P3** Max-Min Scheduler Control Register 2 of Queue 5/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000137C **MMSCR3_Q5P3** Max-Min Scheduler Control Register 3 of Queue 5/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P3

																R_Q5_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001380 MMSCR2_Q6P3 Max-Min Scheduler Control Register 2 of Queue 6/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001384 MMSCR3_Q6P3 Max-Min Scheduler Control Register 3 of Queue 6/Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001388 **MMSCR2_Q7P3** **Max-Min Scheduler Control Register 2 of Queue 7/Port 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P3	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000138C **MMSCR3_Q7P3** **Max-Min Scheduler Control Register 3 of Queue 7/Port 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P3
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P3	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001390 **MMSCR_P3** **Max-Min Scheduler Control Register of Port 3** **00000001**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P3
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P3	When this bit is disabled, the rate limit acts like a leaky bucket principle. Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

00001400 MMSCRO_Q0P4 Max-Min Scheduler Control Register 0 of Queue 00000000

0/Port 4

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P4				MIN_RATE_CTRL_EXP_TB_T_Q0_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P4	Port 4 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P4	Port 4 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 0 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 0 min. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001404 **MMSCR1_Q0P4** Max-Min Scheduler Control Register 1 of Queue 0/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P4				MAX_WEIGHT_Q0_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P4				MAX_RATE_CTRL_EXP_TB_T_Q0_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P4	Port 4 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P4	Port 4 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P4	Port 4 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 0 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 0 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001408 **MMSCR0_Q1P4** Max-Min Scheduler Control Register 0 of Queue 1/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR															

	_Q1_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P4				MIN_RATE_CTRL_EXP_TB_T_Q1_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P4	Port 4 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P4	Port 4 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 1 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000140C **MMSCR1_Q1P4** Max-Min Scheduler Control Register 1 of Queue 1/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P4				MAX_WEIGHT_Q1_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P4				MAX_RATE_CTRL_EXP_TB_T_Q1_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P4	Port 4 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P4	Port 4 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P4	Port 4 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 1 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 1 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001410 **MMSCRO_Q2P4** Max-Min Scheduler Control Register 0 of Queue 2/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P4				MIN_RATE_CTRL_EXP_TB_T_Q2_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P4	Port 4 Queue 2 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P4	Port 4 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 2 min. shaper rate limit control, value range: 0..5

Bit(s)	Name	Description
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P4	When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001414 MMSCR1_Q2P4 Max-Min Scheduler Control Register 1 of Queue 2/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P4				MAX_WEIGHT_Q2_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P4				MAX_RATE_CTRL_EXP_TB_T_Q2_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P4	Port 4 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P4	Port 4 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P4	Port 4 Queue 2 max. shaper rate limit control is enabled 0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001418

MMSCRO_Q3P4

Max-Min Scheduler Control Register 0 of Queue
3/Port 4

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P4				MIN_RATE_CTRL_EXP_TB_T_Q3_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P4	Port 4 Queue 3 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P4	Port 4 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 3 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000141C

MMSCR1_Q3P4

Max-Min Scheduler Control Register 1 of Queue
3/Port 4

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P4				MAX_WEIGHT_Q3_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P4				MAX_RATE_CTRL_EXP_TB_T_Q3_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P4							

Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P4	Port 4 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P4	Port 4 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P4	Port 4 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001420 MMSCR0_Q4P4

Max-Min Scheduler Control Register 0 of Queue 4/Port 4

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P4				MIN_RATE_CTRL_EXP_TB_T_Q4_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P4	Port 4 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P4	Port 4 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001424 **MMSCR1_Q4P4** Max-Min Scheduler Control Register 1 of Queue 4/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P4				MAX_WEIGHT_Q4_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P4				MAX_RATE_CTRL_EXP_TB_T_Q4_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q4_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P4	Port 4 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P4	Port 4 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P4	Port 4 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

Bit(s)	Name	Description

00001428 MMSCRO_Q5P4 Max-Min Scheduler Control Register 0 of Queue 5/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P4				MIN_RATE_CTRL_EXP_TB_T_Q5_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q5_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P4	Port 4 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P4	Port 4 Queue 5 min. shaper rate limit control is enabled 0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 5 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000142C MMSCR1_Q5P4 Max-Min Scheduler Control Register 1 of Queue 5/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P4				MAX_WEIGHT_Q5_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MAX_RATE_EN_Q5_P4				MAX_RATE_CTRL_EXP_TB_T_Q5_P4					MAX_RATE_CTRL_MAN_TB_CBS_Q5_P4						
Type	RW				RW					RW						
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P4	Port 4 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P4	Port 4 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P4	Port 4 Queue 5 max. shaper rate limit control is enabled 0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 5 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001430 **MMSCRO_Q6P4** Max-Min Scheduler Control Register 0 of Queue 6/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P4				MIN_RATE_CTRL_EXP_TB_T_Q6_P4											
Type	RW				RW											
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P4	Port 4 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P4	Port 4 Queue 6 min. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P4	0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 6 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001434 **MMSCR1_Q6P4** Max-Min Scheduler Control Register 1 of Queue 6/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P4				MAX_WEIGHT_Q6_P4											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P4				MAX_RATE_CTRL_EXP_TB_T_Q6_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P4	Port 4 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P4	Port 4 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P4	Port 4 Queue 6 max. shaper rate limit control is enabled 0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 6 max. shaper rate limit control, value range: 1..255
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001438 **MMSCRO_Q7P4** Max-Min Scheduler Control Register 0 of Queue 7/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P4															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P4				MIN_RATE_CTRL_EXP_TB_T_Q7_P4				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P4	Port 4 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P4	Port 4 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 7 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000143C **MMSCR1_Q7P4** Max-Min Scheduler Control Register 1 of Queue 7/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ				MAX_WEIGHT_Q7_P4											

	_Q7_P4															
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P4				MAX_RATE_CTRL_EXP_TB_T_Q7_P4				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P4							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P4	Port 4 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P4	Port 4 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P4	Port 4 Queue 7 max. shaper rate limit control is enabled 0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P4	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 4 Queue 7 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P4	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 4 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001440 ERLCR_P4 Egress Rate Limit Control Register of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P4	EGC_TB_EN_P4		EGC_RATE_CIR_16_P4	EG_RATE_LIMIT_EXP_P4_EGC_TB_T_P4				EG_RATE_LIMIT_MAN_P4_EGC_TB_CBS_P4							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P4	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = [Egress\ Port\ Rate\ Limitation(bps) / 8 * (1/EGC\_TB\_T) (bps)]$ In MT7531DE, $EGC\_RATE\_CIR = [2 * Egress\ Port\ Rate\ Limitation(bps) / 8 * (1/EGC\_TB\_T) (bps)]$
15	EG_RATE_LIMIT_EN_P4	Port 4 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P4	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	EGC_RATE_CIR_16_P4	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 4 Egress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
11:8	EG_RATE_LIMIT_EXP_P4_EGC_TB_T_P4	
7:0	EG_RATE_LIMIT_MAN_P4_EGC_TB_CBS_P4	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When EGC_TB_EN = 0, mantissa part of Port 4 Egress rate limit control, value range: 1..255 In MT7531AE/BE, $Egress\ Port\ Rate\ Limitation = MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, $Egress\ Port\ Rate\ Limitation = (MAN/2) * 10^{(EXP)} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (EGC\_RATE\_CIR * EGC\_TB\_T, EGC\_TB\_CBS * 512)$

00001450

MMSCR2_Q0P4

Max-Min Scheduler Control Register 2 of Queue
0/Port 4

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001454

MMSCR3_Q0P4

Max-Min Scheduler Control Register 3 of Queue
0/Port 4

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001458

MMSCR2_Q1P4

Max-Min Scheduler Control Register 2 of Queue
1/Port 4

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P4															

Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000145C MMSCR3_Q1P4 Max-Min Scheduler Control Register 3 of Queue 1/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001460 MMSCR2_Q2P4 Max-Min Scheduler Control Register 2 of Queue 2/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q2_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001464 MMSCR3_Q2P4 Max-Min Scheduler Control Register 3 of Queue 2/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001468 MMSCR2_Q3P4 Max-Min Scheduler Control Register 2 of Queue 3/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000146C MMSCR3_Q3P4 Max-Min Scheduler Control Register 3 of Queue 3/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001470 **MMSCR2_Q4P4** Max-Min Scheduler Control Register 2 of Queue 4/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001474 **MMSCR3_Q4P4** Max-Min Scheduler Control Register 3 of Queue 4/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001478 **MMSCR2_Q5P4** Max-Min Scheduler Control Register 2 of Queue 5/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P4

																R_Q5_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000147C MMSCR3_Q5P4 Max-Min Scheduler Control Register 3 of Queue 5/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001480 MMSCR2_Q6P4 Max-Min Scheduler Control Register 2 of Queue 6/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001484 **MMSCR3_Q6P4** Max-Min Scheduler Control Register 3 of Queue 6/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001488 **MMSCR2_Q7P4** Max-Min Scheduler Control Register 2 of Queue 7/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P4	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000148C **MMSCR3_Q7P4** Max-Min Scheduler Control Register 3 of Queue 7/Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P4

																R_Q7_P4
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P4															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P4	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001490 MMSCR_P4 Max-Min Scheduler Control Register of Port 4 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P4
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P4	When this bit is disabled, the rate limit acts like a leaky bucket principle. Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

00001500 MMSCRO_Q0P5 Max-Min Scheduler Control Register 0 of Queue 0/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P5				MIN_RATE_CTRL_EXP_TB_T_Q0_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P5							

Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P5	Port 5 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P5	Port 5 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 0 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 0 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001504 MMSCR1_Q0P5

Max-Min Scheduler Control Register 1 of Queue 0/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q0_P5				MAX_WEIGHT_Q0_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P5				MAX_RATE_CTRL_EXP_TB_T_Q0_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P5	Port 5 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P5	Port 5 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P5	Port 5 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 0 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 0 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001508 **MMSCRO_Q1P5** Max-Min Scheduler Control Register 0 of Queue 1/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P5				MIN_RATE_CTRL_EXP_TB_T_Q1_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P5	Port 5 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P5	Port 5 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 1 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000150C

MMSCR1_Q1P5

Max-Min Scheduler Control Register 1 of Queue
1/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P5				MAX_WEIGHT_Q1_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P5				MAX_RATE_CTRL_EXP_TB_T_Q1_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P5	Port 5 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P5	Port 5 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P5	Port 5 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 1 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 1 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001510

MMSCR0_Q2P5

Max-Min Scheduler Control Register 0 of Queue
2/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MIN_RATE_EN_Q2_P5				MIN_RATE_CTRL_EXP_TB_T_Q2_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P5	Port 5 Queue 2 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P5	Port 5 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 2 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001514 **MMSCR1_Q2P5** Max-Min Scheduler Control Register 1 of Queue 2/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P5				MAX_WEIGHT_Q2_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P5				MAX_RATE_CTRL_EXP_TB_T_Q2_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P5	Port 5 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P5	Port 5 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P5	Port 5 Queue 2 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P5	0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001518 MMSCR0_Q3P5

Max-Min Scheduler Control Register 0 of Queue 3/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P5				MIN_RATE_CTRL_EXP_TB_T_Q3_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P5	Port 5 Queue 3 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P5	Port 5 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 3 min. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000151C **MMSCR1_Q3P5** Max-Min Scheduler Control Register 1 of Queue 3/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P5				MAX_WEIGHT_Q3_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P5				MAX_RATE_CTRL_EXP_TB_T_Q3_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P5	Port 5 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P5	Port 5 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P5	Port 5 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001520 **MMSCR0_Q4P5** Max-Min Scheduler Control Register 0 of Queue 4/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR															

	_Q4_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P5				MIN_RATE_CTRL_EXP_TB_T_Q4_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P5	Port 5 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P5	Port 5 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001524 **MMSCR1_Q4P5** Max-Min Scheduler Control Register 1 of Queue 4/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P5				MAX_WEIGHT_Q4_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P5				MAX_RATE_CTRL_EXP_TB_T_Q4_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q4_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P5	Port 5 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P5	Port 5 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P5	Port 5 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001528 **MMSCRO_Q5P5** Max-Min Scheduler Control Register 0 of Queue 5/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q5_P5				MIN_RATE_CTRL_EXP_TB_T_Q5_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q5_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P5	Port 5 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P5	Port 5 Queue 5 min. shaper rate limit control is enabled 0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 5 min. shaper rate limit control, value range: 0..5

Bit(s)	Name	Description
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P5	When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000152C MMSCR1_Q5P5 Max-Min Scheduler Control Register 1 of Queue 5/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P5				MAX_WEIGHT_Q5_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P5				MAX_RATE_CTRL_EXP_TB_T_Q5_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q5_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P5	Port 5 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P5	Port 5 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P5	Port 5 Queue 5 max. shaper rate limit control is enabled 0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 5 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001530

MMSCRO_Q6P5

Max-Min Scheduler Control Register 0 of Queue
6/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P5				MIN_RATE_CTRL_EXP_TB_T_Q6_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q6_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P5	Port 5 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P5	Port 5 Queue 6 min. shaper rate limit control is enabled 0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 6 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001534

MMSCR1_Q6P5

Max-Min Scheduler Control Register 1 of Queue
6/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P5				MAX_WEIGHT_Q6_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P5				MAX_RATE_CTRL_EXP_TB_T_Q6_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P5							

Type	RW					RW										
Reset	0					0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P5	Port 5 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P5	Port 5 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P5	Port 5 Queue 6 max. shaper rate limit control is enabled 0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 6 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001538 MMSCR0_Q7P5

Max-Min Scheduler Control Register 0 of Queue 7/Port 5

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q7_P5															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P5				MIN_RATE_CTRL_EXP_TB_T_Q7_P5				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P5	Port 5 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P5	Port 5 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 7 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000153C **MMSCR1_Q7P5** Max-Min Scheduler Control Register 1 of Queue 7/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P5				MAX_WEIGHT_Q7_P5											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P5				MAX_RATE_CTRL_EXP_TB_T_Q7_P5				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P5							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P5	Port 5 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P5	Port 5 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P5	Port 5 Queue 7 max. shaper rate limit control is enabled 0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P5	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 5 Queue 7 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P5	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 5 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

Bit(s)	Name	Description

00001540 ERLCR_P5 Egress Rate Limit Control Register of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	EGC_RATE_CIR_15_0_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	EG_RATE_LIMIT_EN_P5	EGC_TB_EN_P5		EGC_RATE_CIR_16_P5	EG_RATE_LIMIT_EXP_P5_EGC_TB_T_P5				EG_RATE_LIMIT_MAN_P5_EGC_TB_CBS_P5							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P5	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = [Egress\ Port\ Rate\ Limitation(bps) / 8 * (1/EGC\_TB\_T) (bps)]$ In MT7531DE, $EGC\_RATE\_CIR = [2 * Egress\ Port\ Rate\ Limitation(bps) / 8 * (1/EGC\_TB\_T) (bps)]$
15	EG_RATE_LIMIT_EN_P5	Port 5 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P5	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	EGC_RATE_CIR_16_P5	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 5 Egress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms
11:8	EG_RATE_LIMIT_EXP_P5_EGC_TB_T_P5	

Bit(s)	Name	Description
		8: 2ms
		9: 4ms
		10: 8ms
		11: 16ms
		12: 32ms
		13: 64ms
		14: 128ms
7:0	EG_RATE_LIMIT_MAN_P5_EGC_TB_CBS_P5	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When EGC_TB_EN = 0, mantissa part of Port 5 Egress rate limit control, value range: 1..255 In MT7531AE/BE, Egress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Egress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001550 **MMSCR2_Q0P5** Max-Min Scheduler Control Register 2 of Queue 0/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001554 **MMSCR3_Q0P5** Max-Min Scheduler Control Register 3 of Queue 0/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001558 **MMSCR2_Q1P5** Max-Min Scheduler Control Register 2 of Queue 1/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000155C **MMSCR3_Q1P5** Max-Min Scheduler Control Register 3 of Queue 1/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001560 **MMSCR2_Q2P5** Max-Min Scheduler Control Register 2 of Queue 2/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P5

																R_Q2_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001564 MMSCR3_Q2P5 Max-Min Scheduler Control Register 3 of Queue 2/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001568 MMSCR2_Q3P5 Max-Min Scheduler Control Register 2 of Queue 3/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000156C **MMSCR3_Q3P5** Max-Min Scheduler Control Register 3 of Queue 3/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001570 **MMSCR2_Q4P5** Max-Min Scheduler Control Register 2 of Queue 4/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001574 **MMSCR3_Q4P5** Max-Min Scheduler Control Register 3 of Queue 4/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P5

																R_Q4_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001578 MMSCR2_Q5P5 Max-Min Scheduler Control Register 2 of Queue 5/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000157C MMSCR3_Q5P5 Max-Min Scheduler Control Register 3 of Queue 5/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001580 **MMSCR2_Q6P5** Max-Min Scheduler Control Register 2 of Queue 6/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001584 **MMSCR3_Q6P5** Max-Min Scheduler Control Register 3 of Queue 6/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001588 **MMSCR2_Q7P5** Max-Min Scheduler Control Register 2 of Queue 7/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P5

																R_Q7_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P5	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000158C MMSCR3_Q7P5 Max-Min Scheduler Control Register 3 of Queue 7/Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P5
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P5	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001590 MMSCR_P5 Max-Min Scheduler Control Register of Port 5 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P5
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P5	When this bit is disabled, the rate limit acts like a leaky bucket principle.

Bit(s)	Name	Description
		Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

00001600 MMSCRO_Q0P6 Max-Min Scheduler Control Register 0 of Queue 0/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q0_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q0_P6				MIN_RATE_CTRL_EXP_TB_T_Q0_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q0_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q0_P6	Port 6 Queue 0 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q0_P6	Port 6 Queue 0 min. shaper rate limit control is enabled 0: Queue 0 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q0_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 0 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q0_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 0 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001604 MMSCR1_Q0P6 Max-Min Scheduler Control Register 1 of Queue 0/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ				MAX_WEIGHT_Q0_P6											

	_Q0_P6															
Type	RW															
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q0_P6				MAX_RATE_CTRL_EXP_TB_T_Q0_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q0_P6							
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q0_P6	Port 6 Queue 0 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q0_P6	Port 6 Queue 0 weighted value for max. WFQ weighted value is (q0_max_weight+1'b1)
15	MAX_RATE_EN_Q0_P6	Port 6 Queue 0 max. shaper rate limit control is enabled 0: Queue 0 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 0 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q0_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 0 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q0_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 0 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001608 **MMSCRO_Q1P6** Max-Min Scheduler Control Register 0 of Queue 1/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q1_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q1_P6				MIN_RATE_CTRL_EXP_TB_T_Q1_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q1_P6							
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q1_P6	Port 6 Queue 1 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q1_P6	Port 6 Queue 1 min. shaper rate limit control is enabled 0: Queue 1 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q1_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 1 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q1_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 1 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000160C **MMSCR1_Q1P6** **Max-Min Scheduler Control Register 1 of Queue 1/Port 6** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q1_P6				MAX_WEIGHT_Q1_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q1_P6				MAX_RATE_CTRL_EXP_TB_T_Q1_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q1_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q1_P6	Port 6 Queue 1 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q1_P6	Port 6 Queue 1 weighted value for max. WFQ weighted value is (q1_max_weight+1'b1)
15	MAX_RATE_EN_Q1_P6	Port 6 Queue 1 max. shaper rate limit control is enabled 0: Queue 1 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 1 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q1_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 1 max. shaper rate limit control, value range: 0..5

Bit(s)	Name	Description
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q1_P6	When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14 Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 1 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001610 MMSCRO_Q2P6 Max-Min Scheduler Control Register 0 of Queue 2/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q2_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q2_P6				MIN_RATE_CTRL_EXP_TB_T_Q2_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q2_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q2_P6	Port 6 Queue 2 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q2_P6	Port 6 Queue 2 min. shaper rate limit control is enabled 0: Queue 2 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q2_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 2 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q2_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 2 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001614 MMSCR1_Q2P6 Max-Min Scheduler Control Register 1 of Queue 2/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q2_P6				MAX_WEIGHT_Q2_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q2_P6				MAX_RATE_CTRL_EXP_TB_T_Q2_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q2_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q2_P6	Port 6 Queue 2 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q2_P6	Port 6 Queue 2 weighted value for max. WFQ weighted value is (q2_max_weight+1'b1)
15	MAX_RATE_EN_Q2_P6	Port 6 Queue 2 max. shaper rate limit control is enabled 0: Queue 2 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 2 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q2_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 2 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q2_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 2 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001618 MMSCRO_Q3P6 Max-Min Scheduler Control Register 0 of Queue 3/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q3_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q3_P6				MIN_RATE_CTRL_EXP_TB_T_Q3_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q3_P6							

Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q3_P6	Port 6 Queue 3 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q3_P6	Port 6 Queue 3 min. shaper rate limit control is enabled 0: Queue 3 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q3_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 3 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q3_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 3 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000161C MMSCR1_Q3P6

Max-Min Scheduler Control Register 1 of Queue
3/Port 6

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q3_P6				MAX_WEIGHT_Q3_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q3_P6				MAX_RATE_CTRL_EXP_TB_T_Q3_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q3_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q3_P6	Port 6 Queue 3 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q3_P6	Port 6 Queue 3 weighted value for max. WFQ weighted value is (q3_max_weight+1'b1)
15	MAX_RATE_EN_Q3_P6	Port 6 Queue 3 max. shaper rate limit control is enabled 0: Queue 3 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 3 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q3_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 3 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q3_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 3 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001620 **MMSCRO_Q4P6** Max-Min Scheduler Control Register 0 of Queue 4/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q4_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q4_P6				MIN_RATE_CTRL_EXP_TB_T_Q4_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q4_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q4_P6	Port 6 Queue 4 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q4_P6	Port 6 Queue 4 min. shaper rate limit control is enabled 0: Queue 4 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q4_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 4 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q4_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 4 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001624

MMSCR1_Q4P6

Max-Min Scheduler Control Register 1 of Queue
4/Port 6

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q4_P6				MAX_WEIGHT_Q4_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q4_P6				MAX_RATE_CTRL_EXP_TB_T_Q4_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q4_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q4_P6	Port 6 Queue 4 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q4_P6	Port 6 Queue 4 weighted value for max. WFQ weighted value is (q4_max_weight+1'b1)
15	MAX_RATE_EN_Q4_P6	Port 6 Queue 4 max. shaper rate limit control is enabled 0: Queue 4 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 4 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q4_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 4 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q4_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 4 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001628

MMSCR0_Q5P6

Max-Min Scheduler Control Register 0 of Queue
5/Port 6

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q5_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	MIN_RATE_EN_Q5_P6				MIN_RATE_CTRL_EXP_TB_T_Q5_P6					MIN_RATE_CTRL_MAN_TB_CBS_Q5_P6						
Type	RW				RW					RW						
Reset	0				0	0	0	0		0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q5_P6	Port 6 Queue 5 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q5_P6	Port 6 Queue 5 min. shaper rate limit control is enabled 0: Queue 5 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q5_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 5 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q5_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 5 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000162C **MMSCR1_Q5P6** Max-Min Scheduler Control Register 1 of Queue 5/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q5_P6															
Type	RW															
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q5_P6															
Type	RW															
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q5_P6	Port 6 Queue 5 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q5_P6	Port 6 Queue 5 weighted value for max. WFQ weighted value is (q5_max_weight+1'b1)
15	MAX_RATE_EN_Q5_P6	Port 6 Queue 5 max. shaper rate limit control is enabled

Bit(s)	Name	Description
11:8	MAX_RATE_CTRL_EXP_TB_T_Q5_P6	0: Queue 5 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 5 max. shaper rate limit control is enabled Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 5 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q5_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 5 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001630 **MMSCRO_Q6P6** Max-Min Scheduler Control Register 0 of Queue 6/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR_Q6_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q6_P6				MIN_RATE_CTRL_EXP_TB_T_Q6_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q6_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q6_P6	Port 6 Queue 6 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q6_P6	Port 6 Queue 6 min. shaper rate limit control is enabled 0: Queue 6 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q6_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 6 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q6_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 6 min. shaper rate limit control, value range: 1..255

Bit(s)	Name	Description
		When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001634 **MMSCR1_Q6P6** Max-Min Scheduler Control Register 1 of Queue 6/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q6_P6				MAX_WEIGHT_Q6_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q6_P6				MAX_RATE_CTRL_EXP_TB_T_Q6_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q6_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q6_P6	Port 6 Queue 6 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q6_P6	Port 6 Queue 6 weighted value for max. WFQ weighted value is (q6_max_weight+1'b1)
15	MAX_RATE_EN_Q6_P6	Port 6 Queue 6 max. shaper rate limit control is enabled 0: Queue 6 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 6 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q6_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 6 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q6_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 6 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001638 **MMSCR0_Q7P6** Max-Min Scheduler Control Register 0 of Queue 7/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MIN_SP_WRR															

	_Q7_P6															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_EN_Q7_P6				MIN_RATE_CTRL_EXP_TB_T_Q7_P6				MIN_RATE_CTRL_MAN_TB_CBS_Q7_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MIN_SP_WRR_Q7_P6	Port 6 Queue 7 min. traffic arbitration scheme 0: Round-Robin (RR) 1: Strict Priority (SP)
15	MIN_RATE_EN_Q7_P6	Port 6 Queue 7 min. shaper rate limit control is enabled 0: Queue 7 min. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 min. shaper rate limit control is enabled
11:8	MIN_RATE_CTRL_EXP_TB_T_Q7_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 7 min. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MIN_RATE_CTRL_MAN_TB_CBS_Q7_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 7 min. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

0000163C MMSCR1_Q7P6

Max-Min Scheduler Control Register 1 of Queue 7/Port 6

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	MAX_SP_WFQ_Q7_P6				MAX_WEIGHT_Q7_P6											
Type	RW				RW											
Reset	0				0	0	0	0								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_EN_Q7_P6				MAX_RATE_CTRL_EXP_TB_T_Q7_P6				MAX_RATE_CTRL_MAN_TB_CBS_Q7_P6							
Type	RW				RW				RW							
Reset	0				0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	MAX_SP_WFQ_Q7_P6	Port 6 Queue 7 max. traffic arbitration scheme 0: Weighted Fair Queuing (WFQ) 1: Strict Priority (SP)
27:24	MAX_WEIGHT_Q7_P6	Port 6 Queue 7 weighted value for max. WFQ weighted value is (q7_max_weight+1'b1)
15	MAX_RATE_EN_Q7_P6	Port 6 Queue 7 max. shaper rate limit control is enabled 0: Queue 7 max. shaper rate limit control is disabled, the shaper will always let the pkt pass (infinite rate) 1: Queue 7 max. shaper rate limit control is enabled
11:8	MAX_RATE_CTRL_EXP_TB_T_Q7_P6	Depend on MIN_MAX_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When MIN_MAX_TB_EN = 0, exponent part of Port 6 Queue 7 max. shaper rate limit control, value range: 0..5 When MIN_MAX_TB_EN = 1, support TB_T period for rate measurement, value range: 0..14
7:0	MAX_RATE_CTRL_MAN_TB_CBS_Q7_P6	Depend on MIN_MAX_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When MIN_MAX_TB_EN = 0, mantissa part of Port 6 Queue 7 max. shaper rate limit control, value range: 1..255 When MIN_MAX_TB_EN = 1, support max. bucket size TB_CBS 512 Bytes stepping

00001640		ERLCR_P6		Egress Rate Limit Control Register of Port 6												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	EGC_RATE_CIR_15_0_P6																
Type	RW																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	EG_RATE_LIMIT_EN_P6	EGC_TB_EN_P6		EGC_RATE_LIMIT_EXP_P6_EGC_TB_T_P6					EG_RATE_LIMIT_MAN_P6_EGC_TB_CBS_P6								
Type	RW	RW		RW	RW				RW								
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:16	EGC_RATE_CIR_15_0_P6	When EGC_TB_EN = 1, total 17 bits EGC_RATE_CIR include EGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $EGC\_RATE\_CIR = \lceil \text{Egress Port Rate Limitation}(\text{bps}) / 8 * (1/EGC\_TB\_T) (\text{bps}) \rceil$ In MT7531DE, $EGC\_RATE\_CIR = \lceil 2 * \text{Egress Port Rate Limitation}(\text{bps}) / 8 * (1/EGC\_TB\_T) (\text{bps}) \rceil$
15	EG_RATE_LIMIT_EN_P6	Port 6 Egress rate limit control is enabled 0: Egress rate limit control disable 1: Enable
14	EGC_TB_EN_P6	When this bit is disabled, the Egress rate control acts like a leaky bucket principle. Otherwise, the Egress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

Bit(s)	Name	Description
12	EGC_RATE_CIR_16_P6	Combined with EGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	EG_RATE_LIMIT_EXP_P6_EGC_TB_T_P6	Depend on EGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When EGC_TB_EN = 0, exponent part of Port 6 Egress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When EGC_TB_EN = 1, support EGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	EG_RATE_LIMIT_MAN_P6_EGC_TB_CBS_P6	Depend on EGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When EGC_TB_EN = 0, mantissa part of Port 6 Egress rate limit control, value range: 1..255 In MT7531AE/BE, Egress Port Rate Limitation = $MAN * 10^{EXP} * 1Kbps$ In MT7531DE, Egress Port Rate Limitation = $(MAN/2) * 10^{EXP} * 1Kbps$ When EGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = Max (EGC_RATE_CIR*EGC_TB_T, EGC_TB_CBS*512)

00001650

MMSCR2_Q0P6

Max-Min Scheduler Control Register 2 of Queue

00000000

0/Port 6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q0_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q0_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q0_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001654 **MMSCR3_Q0P6** Max-Min Scheduler Control Register 3 of Queue 0/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q0_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q0_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q0_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001658 **MMSCR2_Q1P6** Max-Min Scheduler Control Register 2 of Queue 1/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q1_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q1_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q1_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000165C **MMSCR3_Q1P6** Max-Min Scheduler Control Register 3 of Queue 1/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q1_P6

																R_Q1_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q1_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q1_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001660 MMSCR2_Q2P6 Max-Min Scheduler Control Register 2 of Queue 2/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q2_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q2_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q2_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001664 MMSCR3_Q2P6 Max-Min Scheduler Control Register 3 of Queue 2/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q2_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q2_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q2_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001668 **MMSCR2_Q3P6** Max-Min Scheduler Control Register 2 of Queue 3/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q3_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q3_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q3_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000166C **MMSCR3_Q3P6** Max-Min Scheduler Control Register 3 of Queue 3/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q3_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q3_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q3_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001670 **MMSCR2_Q4P6** Max-Min Scheduler Control Register 2 of Queue 4/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q4_P6

																R_Q4_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q4_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q4_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001674 MMSCR3_Q4P6 Max-Min Scheduler Control Register 3 of Queue 4/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q4_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q4_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q4_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001678 MMSCR2_Q5P6 Max-Min Scheduler Control Register 2 of Queue 5/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q5_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q5_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q5_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000167C **MMSCR3_Q5P6** Max-Min Scheduler Control Register 3 of Queue 5/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q5_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q5_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q5_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001680 **MMSCR2_Q6P6** Max-Min Scheduler Control Register 2 of Queue 6/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q6_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q6_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q6_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001684 **MMSCR3_Q6P6** Max-Min Scheduler Control Register 3 of Queue 6/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q6_P6

																R_Q6_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q6_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q6_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001688 MMSCR2_Q7P6 Max-Min Scheduler Control Register 2 of Queue 7/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MIN_RATE_CIR_Q7_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MIN_RATE_CIR_Q7_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MIN_RATE_CIR_Q7_P6	Total 17 bits MIN_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

0000168C MMSCR3_Q7P6 Max-Min Scheduler Control Register 3 of Queue 7/Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																MAX_RATE_CIR_Q7_P6
Type																RW
Reset																0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MAX_RATE_CIR_Q7_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
16:0	MAX_RATE_CIR_Q7_P6	Total 17 bits MAX_RATE_CIR, support 32Kbps stepping CIR cover up to 2.5Gbps

00001690 MMSCR_P6 Max-Min Scheduler Control Register of Port 6 00000001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																MIN_MAX_TB_EN_P6
Type																RW
Reset																1

Bit(s)	Name	Description
0	MIN_MAX_TB_EN_P6	When this bit is disabled, the rate limit acts like a leaky bucket principle. Otherwise, the rate limit uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable

4 Buffer Management Unit (BMU)

4.1 Introduction

A total of 1536 memory blocks (pages) are used to store frames in PB_CTRL, which are managed and processed in Buffer Management Unit (BMU). The key concept is the use of linking lists to maintain these blocks.

Before receiving a frame, RX_CTRL will request memory blocks to store the frame. If multiple blocks are used for a specific frame, the interconnections among these blocks are kept inside BMU as page linkers. After the frame is fully received, ARL will determine the egress ports of this frame by looking up its contents. Thus, BMU will store the 1st page linker (called frame linker) of this frame into the corresponding egress queues of egress ports. Once the egress queues of an egress port are not empty, the Scheduler (SCH) will get a frame linker from BMU and then inform the corresponding TX_CTRL to pop data from that page in PB_CTRL.

BMU also supports the flow control (FC) and the priority flow control (PFC) mechanisms. Once the flow control is enabled, there will be no packet dropped in this switch. Besides, the port-based ingress rate limit is also implemented in BMU. To support the TRTCM (Two-Rate Three-Color Meter) function in ARL, drop profiles for different drop precedence are also provided in BMU.

4.2 Features

- Support 1536 pages, per page is 256 bytes
- Packet buffer size is 3*128K Bytes
- Support 8 egress queues per egress port
- Support the flow control and priority flow control mechanisms
- Support the port-based ingress rate control
- Support the 2-bit drop precedence with different drop profiles

4.3 Block Diagram

This section provides a block diagram to illustrate the main components and functions of BMU.

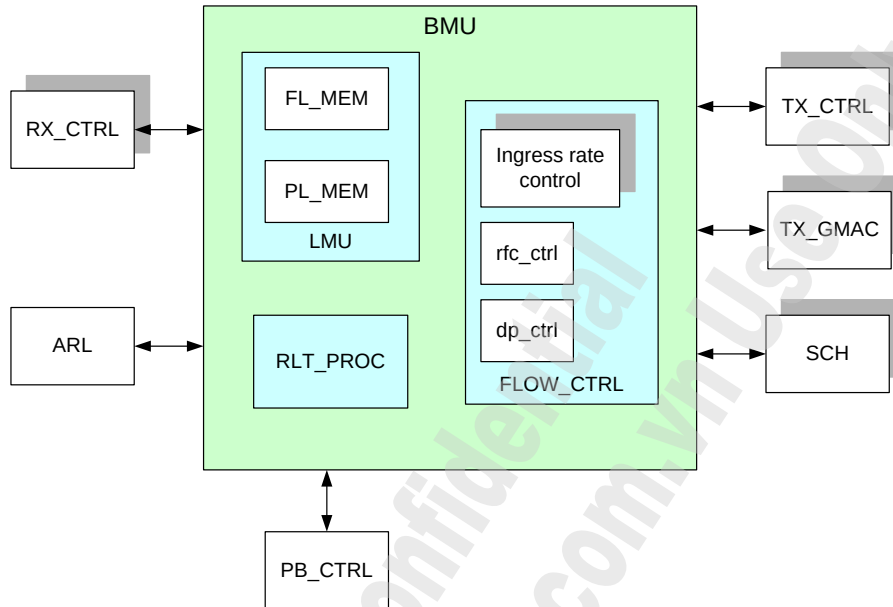


Figure 4-1 Block Diagram of BMU

4.4 Flow Control

4.4.1 Legacy Flow Control

The balance between efficiency and fairness is the key concept of the flow control mechanism. To achieve efficiency, memory pages are allocated for current requirements, and to achieve fairness, pages are reserved for future requirements. The goal for the RFC_CTRL module is that no packet is dropped when flow control is ON. The following figure shows the conditions for flow control ON and OFF. The blue regions are flow control OFF, and the red regions are ON. However, the green region acts as ON when the page conditions change from blue to red, and it acts as OFF when the page conditions change from red to blue.

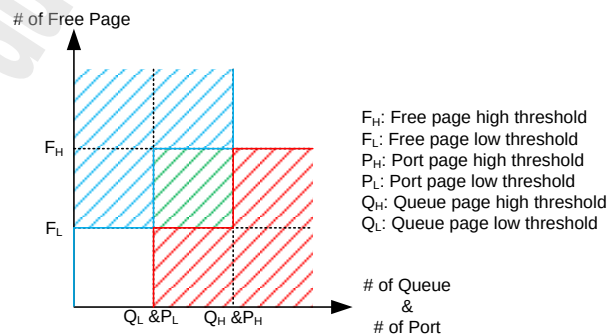


Figure 4-2 Flow Control Profile

4.4.2 Priority Flow Control

In MT7531, it supports IEEE 802.1Qbb priority flow control (PFC) which extends the granularity of IEEE 802.3x PAUSE. When a buffer threshold is exceeded due to congestion, IEEE 802.3x PAUSE sends a pause frame to its peer to pause all data transmission on the link for a specified period of time. However, PFC sends a pause frame that indicates which specific user priority needs to be paused. Using PFC allows administrators to allocate resources, including buffers and queues, based on user priority, which results in a higher level of service for critical traffic where congestion has the greatest effect. The following figure shows the difference between FC and PFC. User priority 4 receives PFC pause frame and stops to send packets due to its peer buffer congestion.

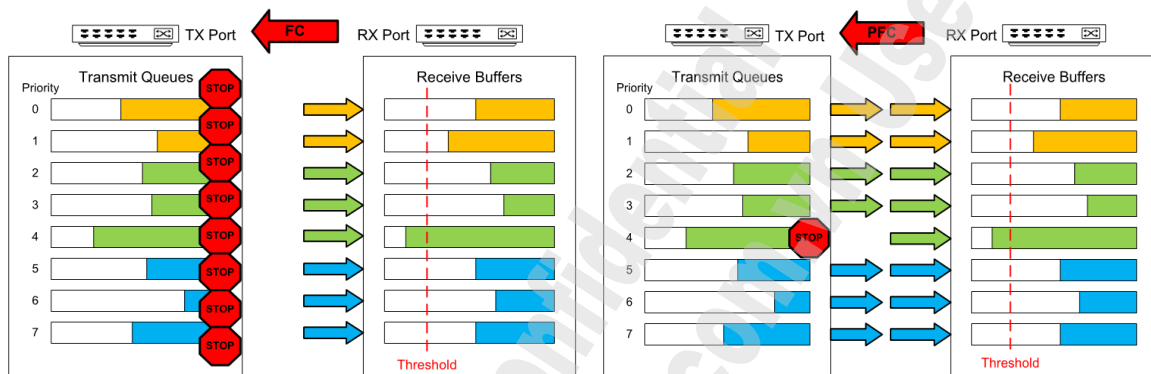


Figure 4-3 Priority Flow Control

4.5 Register Definition

4.5.1 BMU_FC Register

Module name: BMU_FC Base address: (+0x0000)

Address	Name	Width	Register Function
00001800	<u>IRLCR_P0</u>	32	Ingress Rate Limit Control Register of Port 0
00001804	<u>FPC_RXCTRL_P0</u>	32	Free Page Count at RX_CTRL of Port 0
0000180C	<u>MMDPR_10_Q0P0</u>	32	Drop Precedence control 10 of Q0 Port 0
00001810	<u>MMDPR_10_Q1P0</u>	32	Drop Precedence control 10 of Q1 Port 0
00001814	<u>MMDPR_10_Q2P0</u>	32	Drop Precedence control 10 of Q2 Port 0
00001818	<u>MMDPR_10_Q3P0</u>	32	Drop Precedence control 10 of Q3 Port 0
0000181C	<u>MMDPR_10_Q4P0</u>	32	Drop Precedence control 10 of Q4 Port 0
00001820	<u>MMDPR_10_Q5P0</u>	32	Drop Precedence control 10 of Q5 Port 0
00001824	<u>MMDPR_10_Q6P0</u>	32	Drop Precedence control 10 of Q6 Port 0
00001828	<u>MMDPR_10_Q7P0</u>	32	Drop Precedence control 10 of Q7 Port 0
0000182C	<u>MMDPR_11_Q0P0</u>	32	Drop Precedence control 11 of Q0 Port 0
00001830	<u>MMDPR_11_Q1P0</u>	32	Drop Precedence control 11 of Q1 Port 0
00001834	<u>MMDPR_11_Q2P0</u>	32	Drop Precedence control 11 of Q2 Port 0
00001838	<u>MMDPR_11_Q3P0</u>	32	Drop Precedence control 11 of Q3 Port 0
0000183C	<u>MMDPR_11_Q4P0</u>	32	Drop Precedence control 11 of Q4 Port 0
00001840	<u>MMDPR_11_Q5P0</u>	32	Drop Precedence control 11 of Q5 Port 0
00001844	<u>MMDPR_11_Q6P0</u>	32	Drop Precedence control 11 of Q6 Port 0

00001848	<u>MMDPR 11_Q7P0</u>	32	Drop Precedence control 11 of Q7 Port 0
00001900	<u>IRLCR_P1</u>	32	Ingress Rate Limit Control Register of Port 1
00001904	<u>FPC_RXCTRL_P1</u>	32	Free Page Count at RX_CTRL of Port 1
0000190C	<u>MMDPR 10_Q0P1</u>	32	Drop Precedence control 10 of Q0 Port 1
00001910	<u>MMDPR 10_Q1P1</u>	32	Drop Precedence control 10 of Q1 Port 1
00001914	<u>MMDPR 10_Q2P1</u>	32	Drop Precedence control 10 of Q2 Port 1
00001918	<u>MMDPR 10_Q3P1</u>	32	Drop Precedence control 10 of Q3 Port 1
0000191C	<u>MMDPR 10_Q4P1</u>	32	Drop Precedence control 10 of Q4 Port 1
00001920	<u>MMDPR 10_Q5P1</u>	32	Drop Precedence control 10 of Q5 Port 1
00001924	<u>MMDPR 10_Q6P1</u>	32	Drop Precedence control 10 of Q6 Port 1
00001928	<u>MMDPR 10_Q7P1</u>	32	Drop Precedence control 10 of Q7 Port 1
0000192C	<u>MMDPR 11_Q0P1</u>	32	Drop Precedence control 11 of Q0 Port 1
00001930	<u>MMDPR 11_Q1P1</u>	32	Drop Precedence control 11 of Q1 Port 1
00001934	<u>MMDPR 11_Q2P1</u>	32	Drop Precedence control 11 of Q2 Port 1
00001938	<u>MMDPR 11_Q3P1</u>	32	Drop Precedence control 11 of Q3 Port 1
0000193C	<u>MMDPR 11_Q4P1</u>	32	Drop Precedence control 11 of Q4 Port 1
00001940	<u>MMDPR 11_Q5P1</u>	32	Drop Precedence control 11 of Q5 Port 1
00001944	<u>MMDPR 11_Q6P1</u>	32	Drop Precedence control 11 of Q6 Port 1
00001948	<u>MMDPR 11_Q7P1</u>	32	Drop Precedence control 11 of Q7 Port 1
00001A00	<u>IRLCR_P2</u>	32	Ingress Rate Limit Control Register of Port 2
00001A04	<u>FPC_RXCTRL_P2</u>	32	Free Page Count at RX_CTRL of Port 2
00001A0C	<u>MMDPR 10_Q0P2</u>	32	Drop Precedence control 10 of Q0 Port 2
00001A10	<u>MMDPR 10_Q1P2</u>	32	Drop Precedence control 10 of Q1 Port 2
00001A14	<u>MMDPR 10_Q2P2</u>	32	Drop Precedence control 10 of Q2 Port 2
00001A18	<u>MMDPR 10_Q3P2</u>	32	Drop Precedence control 10 of Q3 Port 2
00001A1C	<u>MMDPR 10_Q4P2</u>	32	Drop Precedence control 10 of Q4 Port 2
00001A20	<u>MMDPR 10_Q5P2</u>	32	Drop Precedence control 10 of Q5 Port 2
00001A24	<u>MMDPR 10_Q6P2</u>	32	Drop Precedence control 10 of Q6 Port 2
00001A28	<u>MMDPR 10_Q7P2</u>	32	Drop Precedence control 10 of Q7 Port 2
00001A2C	<u>MMDPR 11_Q0P2</u>	32	Drop Precedence control 11 of Q0 Port 2
00001A30	<u>MMDPR 11_Q1P2</u>	32	Drop Precedence control 11 of Q1 Port 2
00001A34	<u>MMDPR 11_Q2P2</u>	32	Drop Precedence control 11 of Q2 Port 2
00001A38	<u>MMDPR 11_Q3P2</u>	32	Drop Precedence control 11 of Q3 Port 2
00001A3C	<u>MMDPR 11_Q4P2</u>	32	Drop Precedence control 11 of Q4 Port 2
00001A40	<u>MMDPR 11_Q5P2</u>	32	Drop Precedence control 11 of Q5 Port 2
00001A44	<u>MMDPR 11_Q6P2</u>	32	Drop Precedence control 11 of Q6 Port 2
00001A48	<u>MMDPR 11_Q7P2</u>	32	Drop Precedence control 11 of Q7 Port 2
00001B00	<u>IRLCR_P3</u>	32	Ingress Rate Limit Control Register of Port 3
00001B04	<u>FPC_RXCTRL_P3</u>	32	Free Page Count at RX_CTRL of Port 3
00001B0C	<u>MMDPR 10_Q0P3</u>	32	Drop Precedence control 10 of Q0 Port 3
00001B10	<u>MMDPR 10_Q1P3</u>	32	Drop Precedence control 10 of Q1 Port 3
00001B14	<u>MMDPR 10_Q2P3</u>	32	Drop Precedence control 10 of Q2 Port 3
00001B18	<u>MMDPR 10_Q3P3</u>	32	Drop Precedence control 10 of Q3 Port 3
00001B1C	<u>MMDPR 10_Q4P3</u>	32	Drop Precedence control 10 of Q4 Port 3
00001B20	<u>MMDPR 10_Q5P3</u>	32	Drop Precedence control 10 of Q5 Port 3
00001B24	<u>MMDPR 10_Q6P3</u>	32	Drop Precedence control 10 of Q6 Port 3
00001B28	<u>MMDPR 10_Q7P3</u>	32	Drop Precedence control 10 of Q7 Port 3
00001B2C	<u>MMDPR 11_Q0P3</u>	32	Drop Precedence control 11 of Q0 Port 3
00001B30	<u>MMDPR 11_Q1P3</u>	32	Drop Precedence control 11 of Q1 Port 3
00001B34	<u>MMDPR 11_Q2P3</u>	32	Drop Precedence control 11 of Q2 Port 3

00001B38	<u>MMDPR 11 Q3P3</u>	32	Drop Precedence control 11 of Q3 Port 3
00001B3C	<u>MMDPR 11 Q4P3</u>	32	Drop Precedence control 11 of Q4 Port 3
00001B40	<u>MMDPR 11 Q5P3</u>	32	Drop Precedence control 11 of Q5 Port 3
00001B44	<u>MMDPR 11 Q6P3</u>	32	Drop Precedence control 11 of Q6 Port 3
00001B48	<u>MMDPR 11 Q7P3</u>	32	Drop Precedence control 11 of Q7 Port 3
00001C00	<u>IRLCR P4</u>	32	Ingress Rate Limit Control Register of Port 4
00001C04	<u>FPC RXCTRL P4</u>	32	Free Page Count at RX_CTRL of Port 4
00001C0C	<u>MMDPR 10 Q0P4</u>	32	Drop Precedence control 10 of Q0 Port 4
00001C10	<u>MMDPR 10 Q1P4</u>	32	Drop Precedence control 10 of Q1 Port 4
00001C14	<u>MMDPR 10 Q2P4</u>	32	Drop Precedence control 10 of Q2 Port 4
00001C18	<u>MMDPR 10 Q3P4</u>	32	Drop Precedence control 10 of Q3 Port 4
00001C1C	<u>MMDPR 10 Q4P4</u>	32	Drop Precedence control 10 of Q4 Port 4
00001C20	<u>MMDPR 10 Q5P4</u>	32	Drop Precedence control 10 of Q5 Port 4
00001C24	<u>MMDPR 10 Q6P4</u>	32	Drop Precedence control 10 of Q6 Port 4
00001C28	<u>MMDPR 10 Q7P4</u>	32	Drop Precedence control 10 of Q7 Port 4
00001C2C	<u>MMDPR 11 Q0P4</u>	32	Drop Precedence control 11 of Q0 Port 4
00001C30	<u>MMDPR 11 Q1P4</u>	32	Drop Precedence control 11 of Q1 Port 4
00001C34	<u>MMDPR 11 Q2P4</u>	32	Drop Precedence control 11 of Q2 Port 4
00001C38	<u>MMDPR 11 Q3P4</u>	32	Drop Precedence control 11 of Q3 Port 4
00001C3C	<u>MMDPR 11 Q4P4</u>	32	Drop Precedence control 11 of Q4 Port 4
00001C40	<u>MMDPR 11 Q5P4</u>	32	Drop Precedence control 11 of Q5 Port 4
00001C44	<u>MMDPR 11 Q6P4</u>	32	Drop Precedence control 11 of Q6 Port 4
00001C48	<u>MMDPR 11 Q7P4</u>	32	Drop Precedence control 11 of Q7 Port 4
00001D00	<u>IRLCR P5</u>	32	Ingress Rate Limit Control Register of Port 5
00001D04	<u>FPC RXCTRL P5</u>	32	Free Page Count at RX_CTRL of Port 5
00001D0C	<u>MMDPR 10 Q0P5</u>	32	Drop Precedence control 10 of Q0 Port 5
00001D10	<u>MMDPR 10 Q1P5</u>	32	Drop Precedence control 10 of Q1 Port 5
00001D14	<u>MMDPR 10 Q2P5</u>	32	Drop Precedence control 10 of Q2 Port 5
00001D18	<u>MMDPR 10 Q3P5</u>	32	Drop Precedence control 10 of Q3 Port 5
00001D1C	<u>MMDPR 10 Q4P5</u>	32	Drop Precedence control 10 of Q4 Port 5
00001D20	<u>MMDPR 10 Q5P5</u>	32	Drop Precedence control 10 of Q5 Port 5
00001D24	<u>MMDPR 10 Q6P5</u>	32	Drop Precedence control 10 of Q6 Port 5
00001D28	<u>MMDPR 10 Q7P5</u>	32	Drop Precedence control 10 of Q7 Port 5
00001D2C	<u>MMDPR 11 Q0P5</u>	32	Drop Precedence control 11 of Q0 Port 5
00001D30	<u>MMDPR 11 Q1P5</u>	32	Drop Precedence control 11 of Q1 Port 5
00001D34	<u>MMDPR 11 Q2P5</u>	32	Drop Precedence control 11 of Q2 Port 5
00001D38	<u>MMDPR 11 Q3P5</u>	32	Drop Precedence control 11 of Q3 Port 5
00001D3C	<u>MMDPR 11 Q4P5</u>	32	Drop Precedence control 11 of Q4 Port 5
00001D40	<u>MMDPR 11 Q5P5</u>	32	Drop Precedence control 11 of Q5 Port 5
00001D44	<u>MMDPR 11 Q6P5</u>	32	Drop Precedence control 11 of Q6 Port 5
00001D48	<u>MMDPR 11 Q7P5</u>	32	Drop Precedence control 11 of Q7 Port 5
00001E00	<u>IRLCR P6</u>	32	Ingress Rate Limit Control Register of Port 6
00001E04	<u>FPC RXCTRL P6</u>	32	Free Page Count at RX_CTRL of Port 6
00001E0C	<u>MMDPR 10 Q0P6</u>	32	Drop Precedence control 10 of Q0 Port 6
00001E10	<u>MMDPR 10 Q1P6</u>	32	Drop Precedence control 10 of Q1 Port 6
00001E14	<u>MMDPR 10 Q2P6</u>	32	Drop Precedence control 10 of Q2 Port 6
00001E18	<u>MMDPR 10 Q3P6</u>	32	Drop Precedence control 10 of Q3 Port 6
00001E1C	<u>MMDPR 10 Q4P6</u>	32	Drop Precedence control 10 of Q4 Port 6
00001E20	<u>MMDPR 10 Q5P6</u>	32	Drop Precedence control 10 of Q5 Port 6
00001E24	<u>MMDPR 10 Q6P6</u>	32	Drop Precedence control 10 of Q6 Port 6

00001E28	<u>MMDPR 10_Q7P6</u>	32	Drop Precedence control 10 of Q7 Port 6
00001E2C	<u>MMDPR 11_Q0P6</u>	32	Drop Precedence control 11 of Q0 Port 6
00001E30	<u>MMDPR 11_Q1P6</u>	32	Drop Precedence control 11 of Q1 Port 6
00001E34	<u>MMDPR 11_Q2P6</u>	32	Drop Precedence control 11 of Q2 Port 6
00001E38	<u>MMDPR 11_Q3P6</u>	32	Drop Precedence control 11 of Q3 Port 6
00001E3C	<u>MMDPR 11_Q4P6</u>	32	Drop Precedence control 11 of Q4 Port 6
00001E40	<u>MMDPR 11_Q5P6</u>	32	Drop Precedence control 11 of Q5 Port 6
00001E44	<u>MMDPR 11_Q6P6</u>	32	Drop Precedence control 11 of Q6 Port 6
00001E48	<u>MMDPR 11_Q7P6</u>	32	Drop Precedence control 11 of Q7 Port 6
00001FC0	<u>FPLC</u>	32	Free Page Link Count Register
00001FE0	<u>GFCCR0</u>	32	Global Flow_Control Control Register 0
00001FE4	<u>GFCCR1</u>	32	Global Flow_Control Control Register 1
00001FE8	<u>GFCCR2</u>	32	Global Flow_Control Control Register 2
00001FEC	<u>GFCCR3</u>	32	Global Flow_Control Control Register 3
00001FF0	<u>GFCCR4</u>	32	Global Flow_Control Control Register 4
00001FF4	<u>FCBRCR0</u>	32	Flow Control Block Reservation Control Register
00001FFC	<u>GIRLCR</u>	32	Global Ingress Rate Limit Control Register

00001800 IRLCR_P0 Ingress Rate Limit Control Register of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P0															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P0	IGC_TB_EN_P0		IGC_RATE_CIR_16_P0	IGC_RATE_EXP_P0_IGC_TB_T_P0				IGC_RATE_MAN_P0_IGC_TB_CBS_P0							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P0	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, IGC_RATE_CIR = [Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)] In MT7531DE, IGC_RATE_CIR = [2 * Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)]
15	IGC_RATE_EN_P0	Port 0 Ingress rate limit control is enabled 0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled
14	IGC_TB_EN_P0	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P0	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	IGC_RATE_EXP_P0_IGC_TB_T_P0	Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket

Bit(s)	Name	Description
		When IGC_TB_EN = 0, exponent part of Port 0 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	IGC_RATE_MAN_P0_IGC_TB_CBS_P0	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 0 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, Ingress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Ingress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (IGC\_RATE\_CIR * IGC\_TB\_T, IGC\_TB\_CBS * 512)$

00001804	FPC_RXCTRL_P0				Free Page Count at RX_CTRL of Port 0										00000003		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name														FPC_RXCTRL_P0			
Type														RO			
Reset														0	1	1	

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P0	It indicates the free page count at RX_CTRL module.

0000180C	MMDPR_10_Q0P0	Drop Precedence control 10 of Q0 Port 0	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P0_DP_en					P0Q0_pr_dp10						P0Q0_ht_dp10				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q0_ht_dp10							P0Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P0_DP_en	Enable Drop Precedence function of P0. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth >= P0Q0_ht_dp10, the drop probability of the incoming packet is 100%. (2) When queue depth < P0Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P0Q0_lt_dp10 <= queue depth < P0Q0_ht_dp10, the drop probability of incoming packet is based on the setting P0Q0_pr_dp10. 0: Disable 1: Enable
26:24	P0Q0_pr_dp10	Drop probability of P0 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q0_ht_dp10	High threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size
8:0	P0Q0_lt_dp10	Low threshold of P0 Q0 depth for drop precedence = 2'b10. Unit: page size

00001810 MMDPR_10_Q1P0 Drop Precedence control 10 of Q1 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q1_pr_dp10						P0Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q1_ht_dp10							P0Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q1_pr_dp10	Drop probability of P0 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q1_ht_dp10	High threshold of P0 Q1 depth for drop precedence = 2'b10. Unit: page size

Bit(s)	Name	Description
8:0	POQ1_lt_dp10	Low threshold of P0 Q1 depth for drop precedence = 2'b10. Unit: page size

00001814 MMDPR_10_Q2P0 Drop Precedence control 10 of Q2 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						POQ2_pr_dp10						POQ2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POQ2_ht_dp10								POQ2_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	POQ2_pr_dp10	Drop probability of P0 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	POQ2_ht_dp10	High threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	POQ2_lt_dp10	Low threshold of P0 Q2 depth for drop precedence = 2'b10. Unit: page size

00001818 MMDPR_10_Q3P0 Drop Precedence control 10 of Q3 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						POQ3_pr_dp10						POQ3_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	POQ3_ht_dp10								POQ3_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	POQ3_pr_dp10	Drop probability of P0 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	POQ3_ht_dp10	High threshold of P0 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	POQ3_lt_dp10	Low threshold of P0 Q3 depth for drop precedence = 2'b10. Unit: page size

0000181C MMDPR 10 Q4P0 Drop Precedence control 10 of Q4 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q4_pr_dp10						P0Q4_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q4_ht_dp10								P0Q4_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q4_pr_dp10	Drop probability of P0 Q4 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q4_ht_dp10	High threshold of P0 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P0Q4_lt_dp10	Low threshold of P0 Q4 depth for drop precedence = 2'b10. Unit: page size

00001820 MMDPR 10 Q5P0 Drop Precedence control 10 of Q5 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q5_pr_dp10						P0Q5_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q5_ht_dp10								P0Q5_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q5_pr_dp10	Drop probability of P0 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q5_ht_dp10	High threshold of P0 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P0Q5_lt_dp10	Low threshold of P0 Q5 depth for drop precedence = 2'b10. Unit: page size

00001824 MMDPR 10 Q6P0 Drop Precedence control 10 of Q6 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name						P0Q6_pr_dp10						P0Q6_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q6_ht_dp10								P0Q6_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q6_pr_dp10	Drop probability of P0 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q6_ht_dp10	High threshold of P0 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P0Q6_lt_dp10	Low threshold of P0 Q6 depth for drop precedence = 2'b10. Unit: page size

00001828 MMDPR 10 Q7P0 Drop Precedence control 10 of Q7 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q7_pr_dp10						P0Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q7_ht_dp10								P0Q7_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q7_pr_dp10	Drop probability of P0 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q7_ht_dp10	High threshold of P0 Q7 depth for drop precedence = 2'b10. Unit: page size
8:0	P0Q7_lt_dp10	Low threshold of P0 Q7 depth for drop precedence = 2'b10. Unit: page size

0000182C MMDPR 11 Q0P0 Drop Precedence control 11 of Q0 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q0_pr_dp11						P0Q0_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P0Q0_ht_dp11				P0Q0_lt_dp11										
Type	RW				RW										
Reset	0	0	0	0				0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q0_pr_dp11	Drop probability of P0 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q0_ht_dp11	High threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q0_lt_dp11	Low threshold of P0 Q0 depth for drop precedence = 2'b11. Unit: page size

00001830 MMDPR_11_Q1P0 Drop Precedence control 11 of Q1 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q1_pr_dp11						P0Q1_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q1_ht_dp11							P0Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q1_pr_dp11	Drop probability of P0 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q1_ht_dp11	High threshold of P0 Q1 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q1_lt_dp11	Low threshold of P0 Q1 depth for drop precedence = 2'b11. Unit: page size

00001834 MMDPR_11_Q2P0 Drop Precedence control 11 of Q2 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q2_pr_dp11						P0Q2_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q2_ht_dp11							P0Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q2_pr_dp11	Drop probability of P0 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q2_ht_dp11	High threshold of P0 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q2_lt_dp11	Low threshold of P0 Q2 depth for drop precedence = 2'b11. Unit: page size

00001838 MMDPR_11_Q3P0 Drop Precedence control 11 of Q3 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q3_pr_dp11						P0Q3_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q3_ht_dp11							P0Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q3_pr_dp11	Drop probability of P0 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q3_ht_dp11	High threshold of P0 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q3_lt_dp11	Low threshold of P0 Q3 depth for drop precedence = 2'b11. Unit: page size

0000183C MMDPR_11_Q4P0 Drop Precedence control 11 of Q4 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q4_pr_dp11						P0Q4_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q4_ht_dp11							P0Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q4_pr_dp11	Drop probability of P0 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5%

Bit(s)	Name	Description
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P0Q4_ht_dp11	High threshold of P0 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q4_lt_dp11	Low threshold of P0 Q4 depth for drop precedence = 2'b11. Unit: page size

00001840	MMDPR 11 Q5P0					Drop Precedence control 11 of Q5 Port 0										00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name						P0Q5_pr_dp11							P0Q5_ht_dp11							
Type						RW							RW							
Reset						0	0	0					0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	P0Q5_ht_dp11									P0Q5_lt_dp11										
Type	RW									RW										
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
26:24	P0Q5_pr_dp11	Drop probability of P0 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q5_ht_dp11	High threshold of P0 Q5 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q5_lt_dp11	Low threshold of P0 Q5 depth for drop precedence = 2'b11. Unit: page size

00001844	MMDPR 11 Q6P0					Drop Precedence control 11 of Q6 Port 0											00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16					
Name						PQ06_pr_dp11						PQ06_ht_dp11									
Type						RW						RW									
Reset						0	0	0				0	0	0	0	0					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Name	PQ06_ht_dp11								PQ06_lt_dp11												
Type	RW								RW												
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0					

Bit(s)	Name	Description
26:24	P0Q6_pr_dp11	Drop probability of P0 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P0Q6_ht_dp11	High threshold of P0 Q6 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q6_lt_dp11	Low threshold of P0 Q6 depth for drop precedence = 2'b11. Unit: page size

00001848 MMDPR_11_Q7P0 Drop Precedence control 11 of Q7 Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P0Q7_pr_dp11						P0Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P0Q7_ht_dp11								P0Q7_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P0Q7_pr_dp11	Drop probability of P0 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P0Q7_ht_dp11	High threshold of P0 Q7 depth for drop precedence = 2'b11. Unit: page size
8:0	P0Q7_lt_dp11	Low threshold of P0 Q7 depth for drop precedence = 2'b11. Unit: page size

00001900 IRLCR_P1 Ingress Rate Limit Control Register of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P1	IGC_TB_EN_P1		IGC_RATE_CIR_16_P1	IGC_RATE_EXP_P1_IGC_TB_T_P1				IGC_RATE_MAN_P1_IGC_TB_CBS_P1							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P1	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, IGC_RATE_CIR = [Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)] In MT7531DE, IGC_RATE_CIR = [2 * Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)]
15	IGC_RATE_EN_P1	Port 1 Ingress rate limit control is enabled

Bit(s)	Name	Description
		0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled
14	IGC_TB_EN_P1	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P1	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	IGC_RATE_EXP_P1_IGC_TB_T_P1	Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When IGC_TB_EN = 0, exponent part of Port 1 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	IGC_RATE_MAN_P1_IGC_TB_CBS_P1	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 1 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, Ingress Port Rate Limitation = $MAN \cdot 10^{(EXP)} \cdot 1Kbps$ In MT7531DE, Ingress Port Rate Limitation = $(MAN/2) \cdot 10^{(EXP)} \cdot 1Kbps$ Ingress Port Rate Limitation = $MAN \cdot 10^{(EXP)} \cdot 1Kbps$ When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001904	FPC_RXCTRL_P1				Free Page Count at RX_CTRL of Port 1												00000003	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Name																		FPC_RXCTRL_P1
Type																		RO
Reset																		0 1 1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P1	It indicates the free page count at RX_CTRL module.

0000190C MMDPR_10_Q0P1 Drop Precedence control 10 of Q0 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P1_DP_en					P1Q0_pr_dp10						P1Q0_ht_dp10				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q0_ht_dp10							P1Q0_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P1_DP_en	Enable Drop Precedence function of P1.(If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth >= P1Q0_ht_dp10, the drop probability of the incoming packet is 100%. (2) When queue depth < P1Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P1Q0_lt_dp10 <= queue depth < P1Q0_ht_dp10, the drop probability of incoming packet is based on the setting P1Q0_pr_dp10. 0: Disable 1: Enable
26:24	P1Q0_pr_dp10	Drop probability of P1 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q0_ht_dp10	High threshold of P1 Q0 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q0_lt_dp10	Low threshold of P1 Q0 depth for drop precedence = 2'b10. Unit: page size

00001910 MMDPR_10_Q1P1 Drop Precedence control 10 of Q1 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q1_pr_dp10						P1Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q1_ht_dp10							P1Q1_lt_dp10								
Type	RW							RW								

Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q1_pr_dp10	Drop probability of P1 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q1_ht_dp10	High threshold of P1 Q1 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q1_lt_dp10	Low threshold of P1 Q1 depth for drop precedence = 2'b10. Unit: page size

00001914 MMDPR_10_Q2P1 Drop Precedence control 10 of Q2 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q2_pr_dp10						P1Q2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q2_ht_dp10								P1Q2_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q2_pr_dp10	Drop probability of P1 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q2_ht_dp10	High threshold of P1 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q2_lt_dp10	Low threshold of P1 Q2 depth for drop precedence = 2'b10. Unit: page size

00001918 MMDPR_10_Q3P1 Drop Precedence control 10 of Q3 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q3_pr_dp10						P1Q3_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q3_ht_dp10								P1Q3_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q3_pr_dp10	Drop probability of P1 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q3_ht_dp10	High threshold of P1 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q3_lt_dp10	Low threshold of P1 Q3 depth for drop precedence = 2'b10. Unit: page size

0000191C	<u>MMDPR_10_Q4P1</u>				Drop Precedence control 10 of Q4 Port 1										00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name						P1Q4_pr_dp10						P1Q4_ht_dp10						
Type						RW						RW						
Reset						0	0	0				0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	P1Q4_ht_dp10							P1Q4_lt_dp10										
Type	RW							RW										
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
26:24	P1Q4_pr_dp10	Drop probability of P1 Q4 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q4_ht_dp10	High threshold of P1 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q4_lt_dp10	Low threshold of P1 Q4 depth for drop precedence = 2'b10. Unit: page size

00001920	MMDPR_10_Q5P1					Drop Precedence control 10 of Q5 Port 1											00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name						P1Q5_pr_dp10										P1Q5_ht_dp10				
Type						RW										RW				
Reset						0	0	0						0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	P1Q5_ht_dp10										P1Q5_lt_dp10									
Type	RW										RW									
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
26:24	P1Q5_pr_dp10	Drop probability of P1 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5%

Bit(s)	Name	Description
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P1Q5_ht_dp10	High threshold of P1 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q5_lt_dp10	Low threshold of P1 Q5 depth for drop precedence = 2'b10. Unit: page size

00001924 MMDPR 10_Q6P1 Drop Precedence control 10 of Q6 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q6_pr_dp10						P1Q6_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q6_ht_dp10							P1Q6_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q6_pr_dp10	Drop probability of P1 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q6_ht_dp10	High threshold of P1 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q6_lt_dp10	Low threshold of P1 Q6 depth for drop precedence = 2'b10. Unit: page size

00001928 MMDPR 10_Q7P1 Drop Precedence control 10 of Q7 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q7_pr_dp10						P1Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q7_ht_dp10							P1Q7_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q7_pr_dp10	Drop probability of P1 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P1Q7_ht_dp10	High threshold of P1 Q7 depth for drop precedence = 2'b10. Unit: page size
8:0	P1Q7_lt_dp10	Low threshold of P1 Q7 depth for drop precedence = 2'b10. Unit: page size

0000192C MMDPR 11 Q0P1 Drop Precedence control 11 of Q0 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q0_pr_dp11						P1Q0_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q0_ht_dp11								P1Q0_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q0_pr_dp11	Drop probability of P1 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q0_ht_dp11	High threshold of P1 Q0 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q0_lt_dp11	Low threshold of P1 Q0 depth for drop precedence = 2'b11. Unit: page size

00001930 MMDPR 11 Q1P1 Drop Precedence control 11 of Q1 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q1_pr_dp11						P1Q1_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q1_ht_dp11								P1Q1_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q1_pr_dp11	Drop probability of P1 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q1_ht_dp11	High threshold of P1 Q1 depth for drop precedence = 2'b11. Unit: page size

Bit(s)	Name	Description
8:0	P1Q1_lt_dp11	Low threshold of P1 Q1 depth for drop precedence = 2'b11. Unit: page size

00001934 MMDPR_11_Q2P1 Drop Precedence control 11 of Q2 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q2_pr_dp11						P1Q2_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q2_ht_dp11								P1Q2_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q2_pr_dp11	Drop probability of P1 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q2_ht_dp11	High threshold of P1 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q2_lt_dp11	Low threshold of P1 Q2 depth for drop precedence = 2'b11. Unit: page size

00001938 MMDPR_11_Q3P1 Drop Precedence control 11 of Q3 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q3_pr_dp11						P1Q3_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q3_ht_dp11								P1Q3_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q3_pr_dp11	Drop probability of P1 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q3_ht_dp11	High threshold of P1 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q3_lt_dp11	Low threshold of P1 Q3 depth for drop precedence = 2'b11. Unit: page size

0000193C MMDPR 11 Q4P1 Drop Precedence control 11 of Q4 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q4_pr_dp11						P1Q4_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q4_ht_dp11							P1Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q4_pr_dp11	Drop probability of P1 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q4_ht_dp11	High threshold of P1 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q4_lt_dp11	Low threshold of P1 Q4 depth for drop precedence = 2'b11. Unit: page size

00001940 MMDPR 11 Q5P1 Drop Precedence control 11 of Q5 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q5_pr_dp11						P1Q5_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q5_ht_dp11							P1Q5_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q5_pr_dp11	Drop probability of P1 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q5_ht_dp11	High threshold of P1 Q5 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q5_lt_dp11	Low threshold of P1 Q5 depth for drop precedence = 2'b11. Unit: page size

00001944 MMDPR 11 Q6P1 Drop Precedence control 11 of Q6 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name						P1Q6_pr_dp11						P1Q6_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q6_ht_dp11								P1Q6_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q6_pr_dp11	Drop probability of P1 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q6_ht_dp11	High threshold of P1 Q6 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q6_lt_dp11	Low threshold of P1 Q6 depth for drop precedence = 2'b11. Unit: page size

00001948 MMDPR 11 Q7P1 Drop Precedence control 11 of Q7 Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P1Q7_pr_dp11						P1Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P1Q7_ht_dp11								P1Q7_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P1Q7_pr_dp11	Drop probability of P1 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P1Q7_ht_dp11	High threshold of P1 Q7 depth for drop precedence = 2'b11. Unit: page size
8:0	P1Q7_lt_dp11	Low threshold of P1 Q7 depth for drop precedence = 2'b11. Unit: page size

00001A00 IRLCR P2 Ingress Rate Limit Control Register of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P2															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	IGC_RATE_EN_P2	IGC_TB_EN_P2		IGC_RATE_CIR_16_P2	IGC_RATE_EXP_P2_IGC_TB_T_P2				IGC_RATE_MAN_P2_IGC_TB_CBS_P2							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P2	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $IGC\_RATE\_CIR = \lceil \text{Ingress Port Rate Limitation}(\text{bps}) / 8 * (1/IGC\_TB\_T) (\text{bps}) \rceil$ In MT7531DE, $IGC\_RATE\_CIR = \lceil 2 * \text{Ingress Port Rate Limitation}(\text{bps}) / 8 * (1/IGC\_TB\_T) (\text{bps}) \rceil$
15	IGC_RATE_EN_P2	Port 2 Ingress rate limit control is enabled 0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled
14	IGC_TB_EN_P2	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P2	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	IGC_RATE_EXP_P2_IGC_TB_T_P2	Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When IGC_TB_EN = 0, exponent part of Port 2 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	IGC_RATE_MAN_P2_IGC_TB_CBS_P2	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 2 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, $\text{Ingress Port Rate Limitation} = \text{MAN} * 10^{(\text{EXP})} * 1\text{Kbps}$ In MT7531DE, $\text{Ingress Port Rate Limitation} = (\text{MAN}/2) * 10^{(\text{EXP})} * 1\text{Kbps}$

Bit(s)	Name	Description
		When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = Max (IGC_RATE_CIR*IGC_TB_T, IGC_TB_CBS*512)

00001A04 FPC_RXCTRL_P2 Free Page Count at RX_CTRL of Port 2 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P2		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P2	It indicates the free page count at RX_CTRL module.

00001A0C MMDPR_10_Q0P2 Drop Precedence control 10 of Q0 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P2_DP_en					P2Q0_pr_dp10						P2Q0_ht_dp10				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q0_ht_dp10								P2Q0_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P2_DP_en	Enable Drop Precedence function of P2. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth >= P2Q0_ht_dp10, the drop probability of the incoming packet is 100%. (2) When queue depth < P2Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P2Q0_lt_dp10 <= queue depth < P2Q0_ht_dp10, the drop probability of incoming packet is based on the setting P2Q0_pr_dp10. 0: Disable 1: Enable
26:24	P2Q0_pr_dp10	Drop probability of P2 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q0_ht_dp10	High threshold of P2 Q0 depth for drop precedence = 2'b10. Unit: page size

Bit(s)	Name	Description
8:0	P2Q0_lt_dp10	Low threshold of P2 Q0 depth for drop precedence = 2'b10. Unit: page size

00001A10 MMDPR_10_Q1P2 Drop Precedence control 10 of Q1 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q1_pr_dp10						P2Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q1_ht_dp10								P2Q1_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q1_pr_dp10	Drop probability of P2 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q1_ht_dp10	High threshold of P2 Q1 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q1_lt_dp10	Low threshold of P2 Q1 depth for drop precedence = 2'b10. Unit: page size

00001A14 MMDPR_10_Q2P2 Drop Precedence control 10 of Q2 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q2_pr_dp10						P2Q2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q2_ht_dp10								P2Q2_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q2_pr_dp10	Drop probability of P2 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q2_ht_dp10	High threshold of P2 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q2_lt_dp10	Low threshold of P2 Q2 depth for drop precedence = 2'b10. Unit: page size

00001A18 MMDPR_10_Q3P2 Drop Precedence control 10 of Q3 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q3_pr_dp10						P2Q3_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q3_ht_dp10							P2Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q3_pr_dp10	Drop probability of P2 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q3_ht_dp10	High threshold of P2 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q3_lt_dp10	Low threshold of P2 Q3 depth for drop precedence = 2'b10. Unit: page size

00001A1C MMDPR_10_Q4P2 Drop Precedence control 10 of Q4 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q4_pr_dp10						P2Q4_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q4_ht_dp10							P2Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q4_pr_dp10	Drop probability of P2 Q4 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q4_ht_dp10	High threshold of P2 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q4_lt_dp10	Low threshold of P2 Q4 depth for drop precedence = 2'b10. Unit: page size

00001A20 MMDPR_10_Q5P2 Drop Precedence control 10 of Q5 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name						P2Q5_pr_dp10						P2Q5_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q5_ht_dp10								P2Q5_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q5_pr_dp10	Drop probability of P2 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q5_ht_dp10	High threshold of P2 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q5_lt_dp10	Low threshold of P2 Q5 depth for drop precedence = 2'b10. Unit: page size

00001A24 MMDPR_10_Q6P2 Drop Precedence control 10 of Q6 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q6_pr_dp10						P2Q6_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q6_ht_dp10								P2Q6_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q6_pr_dp10	Drop probability of P2 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q6_ht_dp10	High threshold of P2 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q6_lt_dp10	Low threshold of P2 Q6 depth for drop precedence = 2'b10. Unit: page size

00001A28 MMDPR_10_Q7P2 Drop Precedence control 10 of Q7 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q7_pr_dp10						P2Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P2Q7_ht_dp10				P2Q7_lt_dp10										
Type	RW				RW										
Reset	0	0	0	0											

Bit(s)	Name	Description
26:24	P2Q7_pr_dp10	Drop probability of P2 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q7_ht_dp10	High threshold of P2 Q7 depth for drop precedence = 2'b10. Unit: page size
8:0	P2Q7_lt_dp10	Low threshold of P2 Q7 depth for drop precedence = 2'b10. Unit: page size

00001A2C MMDPR_11_Q0P2 Drop Precedence control 11 of Q0 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q0_pr_dp11					P2Q0_ht_dp11					
Type						RW					RW					
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q0_ht_dp11					P2Q0_lt_dp11										
Type	RW					RW										
Reset	0	0	0	0								0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q0_pr_dp11	Drop probability of P2 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q0_ht_dp11	High threshold of P2 Q0 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q0_lt_dp11	Low threshold of P2 Q0 depth for drop precedence = 2'b11. Unit: page size

00001A30 MMDPR_11_Q1P2 Drop Precedence control 11 of Q1 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q1_pr_dp11					P2Q1_ht_dp11					
Type						RW					RW					
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q1_ht_dp11					P2Q1_lt_dp11										
Type	RW					RW										
Reset	0	0	0	0								0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q1_pr_dp11	Drop probability of P2 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q1_ht_dp11	High threshold of P2 Q1 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q1_lt_dp11	Low threshold of P2 Q1 depth for drop precedence = 2'b11. Unit: page size

00001A34	<u>MMDPR_11_Q2P2</u>					Drop Precedence control 11 of Q2 Port 2								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name						P2Q2_pr_dp11						P2Q2_ht_dp11					
Type						RW						RW					
Reset						0	0	0				0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	P2Q2_ht_dp11							P2Q2_lt_dp11									
Type	RW							RW									
Reset	0	0	0	0			0		0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
26:24	P2Q2_pr_dp11	Drop probability of P2 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q2_ht_dp11	High threshold of P2 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q2_lt_dp11	Low threshold of P2 Q2 depth for drop precedence = 2'b11. Unit: page size

00001A38	MMDPR_11_Q3P2					Drop Precedence control 11 of Q3 Port 2											00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16					
Name					P2Q3_pr_dp11								P2Q3_ht_dp11								
Type					RW								RW								
Reset					000								0000								
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Name	P2Q3_ht_dp11								P2Q3_lt_dp11												
Type	RW								RW												
Reset	0	0	0	0					0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
26:24	P2Q3_pr_dp11	Drop probability of P2 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5%

Bit(s)	Name	Description
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P2Q3_ht_dp11	High threshold of P2 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q3_lt_dp11	Low threshold of P2 Q3 depth for drop precedence = 2'b11. Unit: page size

00001A3C	MMDPR 11 Q4P2					Drop Precedence control 11 of Q4 Port 2										00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name						P2Q4_pr_dp11						P2Q4_ht_dp11								
Type						RW						RW								
Reset						0	0	0					0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	P2Q4_ht_dp11									P2Q4_lt_dp11										
Type	RW									RW										
Reset	0	0	0	0					0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
26:24	P2Q4_pr_dp11	Drop probability of P2 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q4_ht_dp11	High threshold of P2 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q4_lt_dp11	Low threshold of P2 Q4 depth for drop precedence = 2'b11. Unit: page size

00001A40				MMDPR 11 Q5P2				Drop Precedence control 11 of Q5 Port 2								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name						P2Q5_pr_dp11						P2Q5_ht_dp11							
Type						RW						RW							
Reset						0	0	0				0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	P2Q5_ht_dp11							P2Q5_lt_dp11											
Type	RW							RW											
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
26:24	P2Q5_pr_dp11	Drop probability of P2 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P2Q5_ht_dp11	High threshold of P2 Q5 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q5_lt_dp11	Low threshold of P2 Q5 depth for drop precedence = 2'b11. Unit: page size

00001A44 MMDPR_11_Q6P2 Drop Precedence control 11 of Q6 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q6_pr_dp11						P2Q6_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q6_ht_dp11								P2Q6_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q6_pr_dp11	Drop probability of P2 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q6_ht_dp11	High threshold of P2 Q6 depth for drop precedence = 2'b11. Unit: page size
8:0	P2Q6_lt_dp11	Low threshold of P2 Q6 depth for drop precedence = 2'b11. Unit: page size

00001A48 MMDPR_11_Q7P2 Drop Precedence control 11 of Q7 Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P2Q7_pr_dp11						P2Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P2Q7_ht_dp11								P2Q7_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P2Q7_pr_dp11	Drop probability of P2 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P2Q7_ht_dp11	High threshold of P2 Q7 depth for drop precedence = 2'b11. Unit: page size

Bit(s)	Name	Description
8:0	P2Q7_lt_dp11	Low threshold of P2 Q7 depth for drop precedence = 2'b11. Unit: page size

00001B00 IRLCR_P3 Ingress Rate Limit Control Register of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P3															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P3	IGC_TB_EN_P3		IGC_RATE_CIR_16_P3	IGC_RATE_EXP_P3_IGC_TB_T_P3				IGC_RATE_MAN_P3_IGC_TB_CBS_P3							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P3	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, IGC_RATE_CIR = [Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)] In MT7531DE, IGC_RATE_CIR = [2 * Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)]
15	IGC_RATE_EN_P3	Port 3 Ingress rate limit control is enabled 0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled
14	IGC_TB_EN_P3	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P3	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	IGC_RATE_EXP_P3_IGC_TB_T_P3	Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When IGC_TB_EN = 0, exponent part of Port 3 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms

Bit(s)	Name	Description
		8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	IGC_RATE_MAN_P3_IGC_TB_CBS_P3	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 3 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, Ingress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Ingress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (IGC\_RATE\_CIR * IGC\_TB\_T, IGC\_TB\_CBS * 512)$

00001B04 FPC_RXCTRL_P3 Free Page Count at RX_CTRL of Port 3 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P3		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P3	It indicates the free page count at RX_CTRL module.

00001B0C MMDPR_10_Q0P3 Drop Precedence control 10 of Q0 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P3_DP_en					P3Q0_pr_dp10						P3Q0_ht_dp10				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q0_ht_dp10								P3Q0_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P3_DP_en	Enable Drop Precedence function of P3. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth $\geq$ P3Q0_ht_dp10, the drop probability of the incoming packet is 100%.

Bit(s)	Name	Description
		(2) When queue depth < P3Q0_lt_dp10, the drop probability of the incoming packet is 0%.
		(3) When P3Q0_lt_dp10 <= queue depth < P3Q0_ht_dp10, the drop probability of incoming packet is based on the setting P3Q0_pr_dp10.
		0: Disable
		1: Enable
26:24	P3Q0_pr_dp10	Drop probability of P3 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q0_ht_dp10	High threshold of P3 Q0 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q0_lt_dp10	Low threshold of P3 Q0 depth for drop precedence = 2'b10. Unit: page size

00001B10 MMDPR_10_Q1P3 Drop Precedence control 10 of Q1 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q1_pr_dp10						P3Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q1_ht_dp10								P3Q1_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q1_pr_dp10	Drop probability of P3 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q1_ht_dp10	High threshold of P3 Q1 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q1_lt_dp10	Low threshold of P3 Q1 depth for drop precedence = 2'b10. Unit: page size

00001B14 MMDPR_10_Q2P3 Drop Precedence control 10 of Q2 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q2_pr_dp10						P3Q2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q2_ht_dp10								P3Q2_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q2_pr_dp10	Drop probability of P3 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q2_ht_dp10	High threshold of P3 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q2_lt_dp10	Low threshold of P3 Q2 depth for drop precedence = 2'b10. Unit: page size

00001B18 MMDPR 10 Q3P3 Drop Precedence control 10 of Q3 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q3_pr_dp10								P3Q3_ht_dp10		
Type						RW								RW		
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q3_ht_dp10										P3Q3_lt_dp10					
Type	RW										RW					
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q3_pr_dp10	Drop probability of P3 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q3_ht_dp10	High threshold of P3 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q3_lt_dp10	Low threshold of P3 Q3 depth for drop precedence = 2'b10. Unit: page size

00001B1C MMDPR 10 Q4P3 Drop Precedence control 10 of Q4 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q4_pr_dp10								P3Q4_ht_dp10		
Type						RW								RW		
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q4_ht_dp10										P3Q4_lt_dp10					
Type	RW										RW					
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q4_pr_dp10	Drop probability of P3 Q4 for drop precedence = 2'b10. 0x0: 0%

Bit(s)	Name	Description
		0x1: 12.5%
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P3Q4_ht_dp10	High threshold of P3 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q4_lt_dp10	Low threshold of P3 Q4 depth for drop precedence = 2'b10. Unit: page size

00001B20	MMDPR_10_Q5P3					Drop Precedence control 10 of Q5 Port 3								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name						P3Q5_pr_dp10							P3Q5_ht_dp10				
Type						RW							RW				
Reset						0	0	0							0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	P3Q5_ht_dp10								P3Q5_lt_dp10								
Type	RW								RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
26:24	P3Q5_pr_dp10	Drop probability of P3 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q5_ht_dp10	High threshold of P3 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q5_lt_dp10	Low threshold of P3 Q5 depth for drop precedence = 2'b10. Unit: page size

00001B24	MMDPR_10_Q6P3				Drop Precedence control 10 of Q6 Port 3												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name						P3Q6_pr_dp10						P3Q6_ht_dp10								
Type						RW						RW								
Reset						0	0	0				0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	P3Q6_ht_dp10							P3Q6_lt_dp10												
Type	RW							RW												
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
26:24	P3Q6_pr_dp10	Drop probability of P3 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P3Q6_ht_dp10	High threshold of P3 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q6_lt_dp10	Low threshold of P3 Q6 depth for drop precedence = 2'b10. Unit: page size

00001B28 MMDPR 10 Q7P3 Drop Precedence control 10 of Q7 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q7_pr_dp10						P3Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q7_ht_dp10								P3Q7_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q7_pr_dp10	Drop probability of P3 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q7_ht_dp10	High threshold of P3 Q7 depth for drop precedence = 2'b10. Unit: page size
8:0	P3Q7_lt_dp10	Low threshold of P3 Q7 depth for drop precedence = 2'b10. Unit: page size

00001B2C MMDPR 11 Q0P3 Drop Precedence control 11 of Q0 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q0_pr_dp11						P3Q0_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q0_ht_dp11								P3Q0_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q0_pr_dp11	Drop probability of P3 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q0_ht_dp11	High threshold of P3 Q0 depth for drop precedence = 2'b11. Unit: page size

Bit(s)	Name	Description
8:0	P3Q0_lt_dp11	Low threshold of P3 Q0 depth for drop precedence = 2'b11. Unit: page size

00001B30 MMDPR_11_Q1P3 Drop Precedence control 11 of Q1 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q1_pr_dp11						P3Q1_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q1_ht_dp11								P3Q1_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q1_pr_dp11	Drop probability of P3 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q1_ht_dp11	High threshold of P3 Q1 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q1_lt_dp11	Low threshold of P3 Q1 depth for drop precedence = 2'b11. Unit: page size

00001B34 MMDPR_11_Q2P3 Drop Precedence control 11 of Q2 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q2_pr_dp11						P3Q2_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q2_ht_dp11								P3Q2_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q2_pr_dp11	Drop probability of P3 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q2_ht_dp11	High threshold of P3 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q2_lt_dp11	Low threshold of P3 Q2 depth for drop precedence = 2'b11. Unit: page size

00001B38 MMDPR 11 Q3P3 Drop Precedence control 11 of Q3 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q3_pr_dp11						P3Q3_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q3_ht_dp11								P3Q3_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q3_pr_dp11	Drop probability of P3 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q3_ht_dp11	High threshold of P3 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q3_lt_dp11	Low threshold of P3 Q3 depth for drop precedence = 2'b11. Unit: page size

00001B3C MMDPR 11 Q4P3 Drop Precedence control 11 of Q4 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q4_pr_dp11						P3Q4_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q4_ht_dp11								P3Q4_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q4_pr_dp11	Drop probability of P3 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q4_ht_dp11	High threshold of P3 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q4_lt_dp11	Low threshold of P3 Q4 depth for drop precedence = 2'b11. Unit: page size

00001B40 MMDPR 11 Q5P3 Drop Precedence control 11 of Q5 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name						P3Q5_pr_dp11						P3Q5_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q5_ht_dp11								P3Q5_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q5_pr_dp11	Drop probability of P3 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q5_ht_dp11	High threshold of P3 Q5 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q5_lt_dp11	Low threshold of P3 Q5 depth for drop precedence = 2'b11. Unit: page size

00001B44 MMDPR 11 Q6P3 Drop Precedence control 11 of Q6 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q6_pr_dp11						P3Q6_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P3Q6_ht_dp11								P3Q6_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q6_pr_dp11	Drop probability of P3 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q6_ht_dp11	High threshold of P3 Q6 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q6_lt_dp11	Low threshold of P3 Q6 depth for drop precedence = 2'b11. Unit: page size

00001B48 MMDPR 11 Q7P3 Drop Precedence control 11 of Q7 Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P3Q7_pr_dp11						P3Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P3Q7_ht_dp11				P3Q7_lt_dp11										
Type	RW				RW										
Reset	0	0	0	0						0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P3Q7_pr_dp11	Drop probability of P3 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P3Q7_ht_dp11	High threshold of P3 Q7 depth for drop precedence = 2'b11. Unit: page size
8:0	P3Q7_lt_dp11	Low threshold of P3 Q7 depth for drop precedence = 2'b11. Unit: page size

00001C00		IRLCR_P4				Ingress Rate Limit Control Register of Port 4												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	IGC_RATE_CIR_15_0_P4																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	IGC_RATE_EN_P4	IGC_TB_EN_P4		IGC_RATE_CIR_16_P4	IGC_RATE_EXP_P4_IGC_TB_T_P4				IGC_RATE_MAN_P4_IGC_TB_CBS_P4										
Type	RW	RW		RW	RW				RW										
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P4	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, IGC_RATE_CIR = [Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)] In MT7531DE, IGC_RATE_CIR = [2 * Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)]
15	IGC_RATE_EN_P4	Port 4 Ingress rate limit control is enabled 0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled
14	IGC_TB_EN_P4	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P4	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	IGC_RATE_EXP_P4_IGC_TB_T_P4	Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When IGC_TB_EN = 0, exponent part of Port 4 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps

Bit(s)	Name	Description
		3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	IGC_RATE_MAN_P4_IGC_TB_CBS_P4	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 4 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, Ingress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Ingress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (IGC\_RATE\_CIR * IGC\_TB\_T, IGC\_TB\_CBS * 512)$

00001C04		FPC_RXCTRL_P4				Free Page Count at RX_CTRL of Port 4										00000003	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																	
Type																	
Reset																	
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																FPC_RXCTRL_P4	
Type																RO	
Reset															0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P4	It indicates the free page count at RX_CTRL module.

00001C0C		MMDPR_10_Q0P4				Drop Precedence control 10 of Q0 Port 4										00000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P4_DP_en						P4Q0_pr_dp10							P4Q0_ht_dp10			
Type	RW						RW							RW			

Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q0_ht_dp10								P4Q0_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P4_DP_en	Enable Drop Precedence function of P4. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth >= P4Q0_ht_dp10, the drop probability of the incoming packet is 100%. (2) When queue depth < P4Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P4Q0_lt_dp10 <= queue depth < P4Q0_ht_dp10, the drop probability of incoming packet is based on the setting P4Q0_pr_dp10. 0: Disable 1: Enable
26:24	P4Q0_pr_dp10	Drop probability of P4 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n * 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q0_ht_dp10	High threshold of P4 Q0 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q0_lt_dp10	Low threshold of P4 Q0 depth for drop precedence = 2'b10. Unit: page size

00001C10 MMDPR_10_Q1P4 Drop Precedence control 10 of Q1 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q1_pr_dp10						P4Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q1_ht_dp10								P4Q1_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q1_pr_dp10	Drop probability of P4 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n * 12.5% 0x7: 87.5% (n=2~6)
20:12	P4Q1_ht_dp10	High threshold of P4 Q1 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q1_lt_dp10	Low threshold of P4 Q1 depth for drop precedence = 2'b10. Unit: page size

00001C14 MMDPR_10_Q2P4 Drop Precedence control 10 of Q2 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q2_pr_dp10						P4Q2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q2_ht_dp10							P4Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q2_pr_dp10	Drop probability of P4 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q2_ht_dp10	High threshold of P4 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q2_lt_dp10	Low threshold of P4 Q2 depth for drop precedence = 2'b10. Unit: page size

00001C18 MMDPR_10_Q3P4 Drop Precedence control 10 of Q3 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q3_pr_dp10						P4Q3_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q3_ht_dp10							P4Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q3_pr_dp10	Drop probability of P4 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q3_ht_dp10	High threshold of P4 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q3_lt_dp10	Low threshold of P4 Q3 depth for drop precedence = 2'b10. Unit: page size

00001C1C MMDPR_10_Q4P4 Drop Precedence control 10 of Q4 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q4_pr_dp10						P4Q4_ht_dp10				
Type						RW						RW				

Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q4_ht_dp10								P4Q4_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q4_pr_dp10	Drop probability of P4 Q4 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q4_ht_dp10	High threshold of P4 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q4_lt_dp10	Low threshold of P4 Q4 depth for drop precedence = 2'b10. Unit: page size

00001C20 MMDPR_10_Q5P4 Drop Precedence control 10 of Q5 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q5_pr_dp10						P4Q5_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q5_ht_dp10								P4Q5_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q5_pr_dp10	Drop probability of P4 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q5_ht_dp10	High threshold of P4 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q5_lt_dp10	Low threshold of P4 Q5 depth for drop precedence = 2'b10. Unit: page size

00001C24 MMDPR_10_Q6P4 Drop Precedence control 10 of Q6 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q6_pr_dp10						P4Q6_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q6_ht_dp10								P4Q6_lt_dp10							
Type	RW								RW							

Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q6_pr_dp10	Drop probability of P4 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q6_ht_dp10	High threshold of P4 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q6_lt_dp10	Low threshold of P4 Q6 depth for drop precedence = 2'b10. Unit: page size

00001C28 MMDPR 10 Q7P4 Drop Precedence control 10 of Q7 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q7_pr_dp10						P4Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q7_ht_dp10								P4Q7_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q7_pr_dp10	Drop probability of P4 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q7_ht_dp10	High threshold of P4 Q7 depth for drop precedence = 2'b10. Unit: page size
8:0	P4Q7_lt_dp10	Low threshold of P4 Q7 depth for drop precedence = 2'b10. Unit: page size

00001C2C MMDPR 11 Q0P4 Drop Precedence control 11 of Q0 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q0_pr_dp11						P4Q0_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q0_ht_dp11								P4Q0_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q0_pr_dp11	Drop probability of P4 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q0_ht_dp11	High threshold of P4 Q0 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q0_lt_dp11	Low threshold of P4 Q0 depth for drop precedence = 2'b11. Unit: page size

00001C30	MMDPR_11_Q1P4					Drop Precedence control 11 of Q1 Port 4										00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name						P4Q1_pr_dp11						P4Q1_ht_dp11								
Type						RW						RW								
Reset						0	0	0				0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	P4Q1_ht_dp11								P4Q1_lt_dp11											
Type	RW								RW											
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
26:24	P4Q1_pr_dp11	Drop probability of P4 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q1_ht_dp11	High threshold of P4 Q1 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q1_lt_dp11	Low threshold of P4 Q1 depth for drop precedence = 2'b11. Unit: page size

00001C34	MMDPR_11_Q2P4					Drop Precedence control 11 of Q2 Port 4											00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16					
Name						P4Q2_pr_dp11						P4Q2_ht_dp11									
Type						RW						RW									
Reset						0	0	0				0	0	0	0	0					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Name	P4Q2_ht_dp11							P4Q2_lt_dp11													
Type	RW							RW													
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0					

Bit(s)	Name	Description
26:24	P4Q2_pr_dp11	Drop probability of P4 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5%

Bit(s)	Name	Description
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P4Q2_ht_dp11	High threshold of P4 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q2_lt_dp11	Low threshold of P4 Q2 depth for drop precedence = 2'b11. Unit: page size

00001C38 MMDPR 11 Q3P4 Drop Precedence control 11 of Q3 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q3_pr_dp11						P4Q3_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q3_ht_dp11							P4Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q3_pr_dp11	Drop probability of P4 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q3_ht_dp11	High threshold of P4 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q3_lt_dp11	Low threshold of P4 Q3 depth for drop precedence = 2'b11. Unit: page size

00001C3C MMDPR 11 Q4P4 Drop Precedence control 11 of Q4 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q4_pr_dp11						P4Q4_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q4_ht_dp11							P4Q4_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q4_pr_dp11	Drop probability of P4 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P4Q4_ht_dp11	High threshold of P4 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q4_lt_dp11	Low threshold of P4 Q4 depth for drop precedence = 2'b11. Unit: page size

00001C40 MMDPR 11 Q5P4 Drop Precedence control 11 of Q5 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q5_pr_dp11						P4Q5_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q5_ht_dp11								P4Q5_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q5_pr_dp11	Drop probability of P4 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q5_ht_dp11	High threshold of P4 Q5 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q5_lt_dp11	Low threshold of P4 Q5 depth for drop precedence = 2'b11. Unit: page size

00001C44 MMDPR 11 Q6P4 Drop Precedence control 11 of Q6 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q6_pr_dp11						P4Q6_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q6_ht_dp11								P4Q6_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q6_pr_dp11	Drop probability of P4 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q6_ht_dp11	High threshold of P4 Q6 depth for drop precedence = 2'b11. Unit: page size

Bit(s)	Name	Description
8:0	P4Q6_lt_dp11	Low threshold of P4 Q6 depth for drop precedence = 2'b11. Unit: page size

00001C48 MMDPR_11_Q7P4 Drop Precedence control 11 of Q7 Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P4Q7_pr_dp11						P4Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P4Q7_ht_dp11								P4Q7_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P4Q7_pr_dp11	Drop probability of P4 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P4Q7_ht_dp11	High threshold of P4 Q7 depth for drop precedence = 2'b11. Unit: page size
8:0	P4Q7_lt_dp11	Low threshold of P4 Q7 depth for drop precedence = 2'b11. Unit: page size

00001D00 IRLCR_P5 Ingress Rate Limit Control Register of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P5															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P5	IGC_TB_EN_P5		IGC_RATE_CIR_16_P5	IGC_RATE_EXP_P5_IGC_TB_T_P5				IGC_RATE_MAN_P5_IGC_TB_CBS_P5							
Type	RW	RW		RW	RW				RW							
Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P5	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, IGC_RATE_CIR = [Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)] In MT7531DE, IGC_RATE_CIR = [2 * Ingress Port Rate Limitation(bps) / 8 * (1/IGC_TB_T) (bps)]
15	IGC_RATE_EN_P5	Port 5 Ingress rate limit control is enabled 0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled

Bit(s)	Name	Description
14	IGC_TB_EN_P5	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P5	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When IGC_TB_EN = 0, exponent part of Port 5 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
11:8	IGC_RATE_EXP_P5_IGC_TB_T_P5	
7:0	IGC_RATE_MAN_P5_IGC_TB_CBS_P5	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 5 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, Ingress Port Rate Limitation = $MAN * 10^{(EXP)} * 1Kbps$ In MT7531DE, Ingress Port Rate Limitation = $(MAN/2) * 10^{(EXP)} * 1Kbps$ When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and Token Bucket = $Max (IGC\_RATE\_CIR * IGC\_TB\_T, IGC\_TB\_CBS * 512)$

00001D04		FPC_RXCTRL_P5				Free Page Count at RX_CTRL of Port 5										00000003	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name														FPC_RXCTRL_P5			
Type														RO			

Reset																0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P5	It indicates the free page count at RX_CTRL module.

00001D0C MMDPR_10_Q0P5 Drop Precedence control 10 of Q0 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P5_DP_en					P5Q0_pr_dp10						P5Q0_ht_dp10				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q0_ht_dp10								P5Q0_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P5_DP_en	Enable Drop Precedence function of P5. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth $\geq$ P5Q0_ht_dp10, the drop probability of the incoming packet is 100%. (2) When queue depth $<$ P5Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P5Q0_lt_dp10 $\leq$ queue depth $<$ P5Q0_ht_dp10, the drop probability of incoming packet is based on the setting P5Q0_pr_dp10. 0: Disable 1: Enable
26:24	P5Q0_pr_dp10	Drop probability of P5 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: $n \times 12.5\%$ 0x7: 87.5% ($n=2 \sim 6$)
20:12	P5Q0_ht_dp10	High threshold of P5 Q0 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q0_lt_dp10	Low threshold of P5 Q0 depth for drop precedence = 2'b10. Unit: page size

00001D10 MMDPR_10_Q1P5 Drop Precedence control 10 of Q1 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q1_pr_dp10						P5Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q1_ht_dp10								P5Q1_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q1_pr_dp10	Drop probability of P5 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q1_ht_dp10	High threshold of P5 Q1 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q1_lt_dp10	Low threshold of P5 Q1 depth for drop precedence = 2'b10. Unit: page size

00001D14 MMDPR_10_Q2P5 Drop Precedence control 10 of Q2 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q2_pr_dp10						P5Q2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q2_ht_dp10							P5Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q2_pr_dp10	Drop probability of P5 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q2_ht_dp10	High threshold of P5 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q2_lt_dp10	Low threshold of P5 Q2 depth for drop precedence = 2'b10. Unit: page size

00001D18 MMDPR_10_Q3P5 Drop Precedence control 10 of Q3 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q3_pr_dp10						P5Q3_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q3_ht_dp10							P5Q3_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q3_pr_dp10	Drop probability of P5 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5%

Bit(s)	Name	Description
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P5Q3_ht_dp10	High threshold of P5 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q3_lt_dp10	Low threshold of P5 Q3 depth for drop precedence = 2'b10. Unit: page size

00001D1C	MMDPR 10_Q4P5					Drop Precedence control 10 of Q4 Port 5										00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q4_pr_dp10						P5Q4_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q4_ht_dp10							P5Q4_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q4_pr_dp10	Drop probability of P5 Q4 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q4_ht_dp10	High threshold of P5 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q4_lt_dp10	Low threshold of P5 Q4 depth for drop precedence = 2'b10. Unit: page size

00001D20	MMDPR 10_Q5P5					Drop Precedence control 10 of Q5 Port 5										00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q5_pr_dp10						P5Q5_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q5_ht_dp10							P5Q5_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q5_pr_dp10	Drop probability of P5 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P5Q5_ht_dp10	High threshold of P5 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q5_lt_dp10	Low threshold of P5 Q5 depth for drop precedence = 2'b10. Unit: page size

00001D24 MMDPR_10_Q6P5 Drop Precedence control 10 of Q6 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q6_pr_dp10						P5Q6_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q6_ht_dp10								P5Q6_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q6_pr_dp10	Drop probability of P5 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q6_ht_dp10	High threshold of P5 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P5Q6_lt_dp10	Low threshold of P5 Q6 depth for drop precedence = 2'b10. Unit: page size

00001D28 MMDPR_10_Q7P5 Drop Precedence control 10 of Q7 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q7_pr_dp10						P5Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q7_ht_dp10								P5Q7_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q7_pr_dp10	Drop probability of P5 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q7_ht_dp10	High threshold of P5 Q7 depth for drop precedence = 2'b10. Unit: page size

Bit(s)	Name	Description
8:0	P5Q7_lt_dp10	Low threshold of P5 Q7 depth for drop precedence = 2'b10. Unit: page size

00001D2C MMDPR_11_Q0P5 Drop Precedence control 11 of Q0 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q0_pr_dp11						P5Q0_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q0_ht_dp11								P5Q0_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q0_pr_dp11	Drop probability of P5 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q0_ht_dp11	High threshold of P5 Q0 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q0_lt_dp11	Low threshold of P5 Q0 depth for drop precedence = 2'b11. Unit: page size

00001D30 MMDPR_11_Q1P5 Drop Precedence control 11 of Q1 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q1_pr_dp11						P5Q1_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q1_ht_dp11								P5Q1_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q1_pr_dp11	Drop probability of P5 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q1_ht_dp11	High threshold of P5 Q1 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q1_lt_dp11	Low threshold of P5 Q1 depth for drop precedence = 2'b11. Unit: page size

00001D34 MMDPR 11 Q2P5 Drop Precedence control 11 of Q2 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q2_pr_dp11						P5Q2_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q2_ht_dp11							P5Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q2_pr_dp11	Drop probability of P5 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q2_ht_dp11	High threshold of P5 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q2_lt_dp11	Low threshold of P5 Q2 depth for drop precedence = 2'b11. Unit: page size

00001D38 MMDPR 11 Q3P5 Drop Precedence control 11 of Q3 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q3_pr_dp11						P5Q3_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q3_ht_dp11							P5Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q3_pr_dp11	Drop probability of P5 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q3_ht_dp11	High threshold of P5 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q3_lt_dp11	Low threshold of P5 Q3 depth for drop precedence = 2'b11. Unit: page size

00001D3C MMDPR 11 Q4P5 Drop Precedence control 11 of Q4 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name						P5Q4_pr_dp11						P5Q4_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q4_ht_dp11								P5Q4_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q4_pr_dp11	Drop probability of P5 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q4_ht_dp11	High threshold of P5 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q4_lt_dp11	Low threshold of P5 Q4 depth for drop precedence = 2'b11. Unit: page size

00001D40 MMDPR 11 Q5P5 Drop Precedence control 11 of Q5 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q5_pr_dp11						P5Q5_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q5_ht_dp11								P5Q5_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q5_pr_dp11	Drop probability of P5 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q5_ht_dp11	High threshold of P5 Q5 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q5_lt_dp11	Low threshold of P5 Q5 depth for drop precedence = 2'b11. Unit: page size

00001D44 MMDPR 11 Q6P5 Drop Precedence control 11 of Q6 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q6_pr_dp11						P5Q6_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	P5Q6_ht_dp11							P5Q6_lt_dp11							
Type	RW							RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q6_pr_dp11	Drop probability of P5 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q6_ht_dp11	High threshold of P5 Q6 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q6_lt_dp11	Low threshold of P5 Q6 depth for drop precedence = 2'b11. Unit: page size

00001D48 MMDPR_11_Q7P5 Drop Precedence control 11 of Q7 Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P5Q7_pr_dp11						P5Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P5Q7_ht_dp11								P5Q7_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0					0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P5Q7_pr_dp11	Drop probability of P5 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P5Q7_ht_dp11	High threshold of P5 Q7 depth for drop precedence = 2'b11. Unit: page size
8:0	P5Q7_lt_dp11	Low threshold of P5 Q7 depth for drop precedence = 2'b11. Unit: page size

00001E00 IRLCR_P6 Ingress Rate Limit Control Register of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	IGC_RATE_CIR_15_0_P6															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	IGC_RATE_EN_P6	IGC_TB_EN_P6		IGC_RATE_CIR_16_P6	IGC_RATE_EXP_P6_IGC_TB_T_P6				IGC_RATE_MAN_P6_IGC_TB_CBS_P6							
Type	RW	RW		RW	RW				RW							

Reset	0	0		0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	IGC_RATE_CIR_15_0_P6	When IGC_TB_EN = 1, total 17 bits IGC_CIR include IGC_RATE_CIR_16 in bit 12 location, support 32Kbps stepping CIR cover up to 2.5Gbps In MT7531AE/BE, $IGC\_RATE\_CIR = \lceil \text{Ingress Port Rate Limitation}(\text{bps}) / 8 * (1/IGC\_TB\_T) (\text{bps}) \rceil$ In MT7531DE, $IGC\_RATE\_CIR = \lceil 2 * \text{Ingress Port Rate Limitation}(\text{bps}) / 8 * (1/IGC\_TB\_T) (\text{bps}) \rceil$
15	IGC_RATE_EN_P6	Port 6 Ingress rate limit control is enabled 0: Ingress rate limit control is disabled 1: Ingress rate limit control is enabled
14	IGC_TB_EN_P6	When this bit is disabled, the Ingress rate control acts like a leaky bucket principle. Otherwise, the Ingress rate control uses the token bucket method, and this approach guarantees some burst level for TCP transaction. 0: CIR/CBS mode token bucket Disable 1: Token bucket mode Enable
12	IGC_RATE_CIR_16_P6	Combined with IGC_RATE_CIR_15_0 to form a 17 bits CIR value
11:8	IGC_RATE_EXP_P6_IGC_TB_T_P6	Depend on IGC_TB_EN, it can be exponent part for leaky bucket or TB_T period for token bucket When IGC_TB_EN = 0, exponent part of Port 6 Ingress rate limit control, value range: 0..5 0: 1Kbps 1: 10Kbps 2: 100Kbps 3: 1Mbps 4: 10Mbps 5: 100Mbps When IGC_TB_EN = 1, support IGC_TB_T period for rate measurement, value range: 0..14 0: 1/128ms 1: 1/64ms 2: 1/32ms 3: 1/16ms 4: 1/8ms 5: 1/4ms 6: 1/2ms 7: 1ms 8: 2ms 9: 4ms 10: 8ms 11: 16ms 12: 32ms 13: 64ms 14: 128ms
7:0	IGC_RATE_MAN_P6_IGC_TB_CBS_P6	Depend on IGC_TB_EN, it can be mantissa part for leaky bucket or TB_CBS stepping for token bucket When IGC_TB_EN = 0, mantissa part of Port 6 Ingress rate limit control, value range: 1..255 In MT7531AE/BE, $\text{Ingress Port Rate Limitation} = \text{MAN} * 10^{(\text{EXP})} * 1\text{Kbps}$ In MT7531DE, $\text{Ingress Port Rate Limitation} = (\text{MAN}/2) * 10^{(\text{EXP})} * 1\text{Kbps}$ When IGC_TB_EN = 1, support max. bucket size CBS 512 Bytes stepping, and $\text{Token Bucket} = \text{Max} (IGC\_RATE\_CIR * IGC\_TB\_T, IGC\_TB\_CBS * 512)$

00001E04 FPC_RXCTRL_P6 Free Page Count at RX_CTRL of Port 6 00000003

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name														FPC_RXCTRL_P6		
Type														RO		
Reset														0	1	1

Bit(s)	Name	Description
2:0	FPC_RXCTRL_P6	It indicates the free page count at RX_CTRL module.

00001E0C MMDPR_10_Q0P6 Drop Precedence control 10 of Q0 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	P6_DP_en					P6Q0_pr_dp10						P6Q0_ht_dp10				
Type	RW					RW						RW				
Reset	0					0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q0_ht_dp10								P6Q0_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	P6_DP_en	Enable Drop Precedence function of P6. (If the function is enabled, some packets will be dropped no matter the flow control is ON or OFF) (1) When queue depth $\geq$ P6Q0_ht_dp10, the drop probability of the incoming packet is 100%. (2) When queue depth $<$ P6Q0_lt_dp10, the drop probability of the incoming packet is 0%. (3) When P6Q0_lt_dp10 $\leq$ queue depth $<$ P6Q0_ht_dp10, the drop probability of incoming packet is based on the setting P6Q0_pr_dp10. 0: Disable 1: Enable
26:24	P6Q0_pr_dp10	Drop probability of P6 Q0 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: $n * 12.5\%$ 0x7: 87.5% ($n=2 \sim 6$)
20:12	P6Q0_ht_dp10	High threshold of P6 Q0 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q0_lt_dp10	Low threshold of P6 Q0 depth for drop precedence = 2'b10. Unit: page size

00001E10 MMDPR_10_Q1P6 Drop Precedence control 10 of Q1 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q1_pr_dp10						P6Q1_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q1_ht_dp10							P6Q1_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q1_pr_dp10	Drop probability of P6 Q1 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q1_ht_dp10	High threshold of P6 Q1 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q1_lt_dp10	Low threshold of P6 Q1 depth for drop precedence = 2'b10. Unit: page size

00001E14 MMDPR_10_Q2P6 Drop Precedence control 10 of Q2 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q2_pr_dp10						P6Q2_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q2_ht_dp10							P6Q2_lt_dp10								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q2_pr_dp10	Drop probability of P6 Q2 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q2_ht_dp10	High threshold of P6 Q2 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q2_lt_dp10	Low threshold of P6 Q2 depth for drop precedence = 2'b10. Unit: page size

00001E18 MMDPR_10_Q3P6 Drop Precedence control 10 of Q3 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q3_pr_dp10						P6Q3_ht_dp10				
Type						RW						RW				

Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q3_ht_dp10								P6Q3_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q3_pr_dp10	Drop probability of P6 Q3 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q3_ht_dp10	High threshold of P6 Q3 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q3_lt_dp10	Low threshold of P6 Q3 depth for drop precedence = 2'b10. Unit: page size

00001E1C MMDPR_10_Q4P6 Drop Precedence control 10 of Q4 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q4_pr_dp10						P6Q4_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q4_ht_dp10								P6Q4_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q4_pr_dp10	Drop probability of P6 Q4 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q4_ht_dp10	High threshold of P6 Q4 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q4_lt_dp10	Low threshold of P6 Q4 depth for drop precedence = 2'b10. Unit: page size

00001E20 MMDPR_10_Q5P6 Drop Precedence control 10 of Q5 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q5_pr_dp10						P6Q5_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q5_ht_dp10								P6Q5_lt_dp10							
Type	RW								RW							

Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q5_pr_dp10	Drop probability of P6 Q5 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q5_ht_dp10	High threshold of P6 Q5 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q5_lt_dp10	Low threshold of P6 Q5 depth for drop precedence = 2'b10. Unit: page size

00001E24 MMDPR_10_Q6P6 Drop Precedence control 10 of Q6 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q6_pr_dp10						P6Q6_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q6_ht_dp10								P6Q6_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q6_pr_dp10	Drop probability of P6 Q6 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q6_ht_dp10	High threshold of P6 Q6 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q6_lt_dp10	Low threshold of P6 Q6 depth for drop precedence = 2'b10. Unit: page size

00001E28 MMDPR_10_Q7P6 Drop Precedence control 10 of Q7 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q7_pr_dp10						P6Q7_ht_dp10				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q7_ht_dp10								P6Q7_lt_dp10							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q7_pr_dp10	Drop probability of P6 Q7 for drop precedence = 2'b10. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q7_ht_dp10	High threshold of P6 Q7 depth for drop precedence = 2'b10. Unit: page size
8:0	P6Q7_lt_dp10	Low threshold of P6 Q7 depth for drop precedence = 2'b10. Unit: page size

00001E2C MMDPR_11_Q0P6 Drop Precedence control 11 of Q0 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q0_pr_dp11						P6Q0_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q0_ht_dp11							P6Q0_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q0_pr_dp11	Drop probability of P6 Q0 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q0_ht_dp11	High threshold of P6 Q0 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q0_lt_dp11	Low threshold of P6 Q0 depth for drop precedence = 2'b11. Unit: page size

00001E30 MMDPR_11_Q1P6 Drop Precedence control 11 of Q1 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q1_pr_dp11						P6Q1_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q1_ht_dp11							P6Q1_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q1_pr_dp11	Drop probability of P6 Q1 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5%

Bit(s)	Name	Description
		0xn: n* 12.5%
		0x7: 87.5%(n=2~6)
20:12	P6Q1_ht_dp11	High threshold of P6 Q1 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q1_lt_dp11	Low threshold of P6 Q1 depth for drop precedence = 2'b11. Unit: page size

00001E34	MMDPR 11 Q2P6						Drop Precedence control 11 of Q2 Port 6								00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q2_pr_dp11						P6Q2_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q2_ht_dp11							P6Q2_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q2_pr_dp11	Drop probability of P6 Q2 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q2_ht_dp11	High threshold of P6 Q2 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q2_lt_dp11	Low threshold of P6 Q2 depth for drop precedence = 2'b11. Unit: page size

00001E38	MMDPR 11 Q3P6						Drop Precedence control 11 of Q3 Port 6								00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q3_pr_dp11						P6Q3_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q3_ht_dp11							P6Q3_lt_dp11								
Type	RW							RW								
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q3_pr_dp11	Drop probability of P6 Q3 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)

Bit(s)	Name	Description
20:12	P6Q3_ht_dp11	High threshold of P6 Q3 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q3_lt_dp11	Low threshold of P6 Q3 depth for drop precedence = 2'b11. Unit: page size

00001E3C MMDPR_11_Q4P6 Drop Precedence control 11 of Q4 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q4_pr_dp11						P6Q4_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q4_ht_dp11								P6Q4_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q4_pr_dp11	Drop probability of P6 Q4 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q4_ht_dp11	High threshold of P6 Q4 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q4_lt_dp11	Low threshold of P6 Q4 depth for drop precedence = 2'b11. Unit: page size

00001E40 MMDPR_11_Q5P6 Drop Precedence control 11 of Q5 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q5_pr_dp11						P6Q5_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q5_ht_dp11								P6Q5_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q5_pr_dp11	Drop probability of P6 Q5 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q5_ht_dp11	High threshold of P6 Q5 depth for drop precedence = 2'b11. Unit: page size

Bit(s)	Name	Description
8:0	P6Q5_lt_dp11	Low threshold of P6 Q5 depth for drop precedence = 2'b11. Unit: page size

00001E44 MMDPR_11_Q6P6 Drop Precedence control 11 of Q6 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q6_pr_dp11						P6Q6_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q6_ht_dp11								P6Q6_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q6_pr_dp11	Drop probability of P6 Q6 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q6_ht_dp11	High threshold of P6 Q6 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q6_lt_dp11	Low threshold of P6 Q6 depth for drop precedence = 2'b11. Unit: page size

00001E48 MMDPR_11_Q7P6 Drop Precedence control 11 of Q7 Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						P6Q7_pr_dp11						P6Q7_ht_dp11				
Type						RW						RW				
Reset						0	0	0				0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	P6Q7_ht_dp11								P6Q7_lt_dp11							
Type	RW								RW							
Reset	0	0	0	0				0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26:24	P6Q7_pr_dp11	Drop probability of P6 Q7 for drop precedence = 2'b11. 0x0: 0% 0x1: 12.5% 0xn: n* 12.5% 0x7: 87.5%(n=2~6)
20:12	P6Q7_ht_dp11	High threshold of P6 Q7 depth for drop precedence = 2'b11. Unit: page size
8:0	P6Q7_lt_dp11	Low threshold of P6 Q7 depth for drop precedence = 2'b11. Unit: page size

00001FC0 FPLC Free Page Link Count Register 0FFF0600

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					MIN_FREE_PL_CNT											
Type					RO											
Reset					1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FREE_PL_CNT											
Type					RO											
Reset					0	1	1	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
27:16	MIN_FREE_PL_CNT	Minimal Free Page Link Count in LMU from last read access
11:0	FREE_PL_CNT	Free Page Link Count in LMU

00001FE0 GFCCR0 Global Flow_Control Control Register 0 20F000B0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FC_OFF 2ON_O PT	FC_ON 2OFF_ OPT			FC_FREE_BLK_HITHD									
Type			RW	RW			RW									
Reset			1	0			0	0	1	1	1	1	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FC_FREE_BLK_LOTHD									
Type							RW									
Reset							0	0	1	0	1	1	0	0	0	0

Bit(s)	Name	Description
29	FC_OFF2ON_OPT	Flow control assertion option 0: Disable 1: Enable aggressive frame discard option in flow control transition from OFF to ON
28	FC_ON2OFF_OPT	Flow control de-assertion option 0: Disable 1: Enable aggressive frame discard option in flow control transition from ON to OFF
25:16	FC_FREE_BLK_HITHD	High water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)
9:0	FC_FREE_BLK_LOTHD	Low water mark of memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)

00001FE4 GFCCR1 Global Flow_Control Control Register 1 00120008

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name							FC_PORT_BLK_HI_THD									
Type							RW									
Reset							0	0	0	0	0	1	0	0	1	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FC_PORT_BLK_THD									
Type							RW									
Reset							0	0	0	0	0	0	1	0	0	0

Bit(s)	Name	Description
25:16	FC_PORT_BLK_HI_THD	Number of port block high threshold (unit: 2 blocks) associated with packet discard mechanism
9:0	FC_PORT_BLK_THD	Per port memory buffer (in unit of 2 blocks) associated with flow control and packet discard mechanism. (not include reserve block)

00001FE8 GFCCR2 Global Flow_Control Control Register 2 04040404

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FC_BLK_THD_Q3								FC_BLK_THD_Q2					
Type			RW								RW					
Reset			0	0	0	1	0	0			0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FC_BLK_THD_Q1								FC_BLK_THD_Q0					
Type			RW								RW					
Reset			0	0	0	1	0	0			0	0	0	1	0	0

Bit(s)	Name	Description
29:24	FC_BLK_THD_Q3	TX Queue 3 block threshold for flow control
21:16	FC_BLK_THD_Q2	TX Queue 2 block threshold for flow control
13:8	FC_BLK_THD_Q1	TX Queue 1 block threshold for flow control
5:0	FC_BLK_THD_Q0	TX Queue 0 block threshold for flow control

00001FEC GFCCR3 Global Flow_Control Control Register 3 04040404

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name			FC_BLK_THD_Q7								FC_BLK_THD_Q6					
Type			RW								RW					
Reset			0	0	0	1	0	0			0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			FC_BLK_THD_Q5								FC_BLK_THD_Q4					
Type			RW								RW					
Reset			0	0	0	1	0	0			0	0	0	1	0	0

Bit(s)	Name	Description
29:24	FC_BLK_THD_Q7	TX Queue 7 block threshold for flow control
21:16	FC_BLK_THD_Q6	TX Queue 6 block threshold for flow control
13:8	FC_BLK_THD_Q5	TX Queue 5 block threshold for flow control
5:0	FC_BLK_THD_Q4	TX Queue 4 block threshold for flow control

00001FF0 GFCCR4 Global Flow_Control Control Register 4 0000000C

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							FC_QUE_BLK_HI_THD									
Type							RW									
Reset							0	0	0	0	0	0	1	1	0	0

Bit(s)	Name	Description
9:0	FC_QUE_BLK_HI_THD	Number of queue block high threshold (unit: 2 blocks) associated with packet discard mechanism

00001FF4 FCBRCR0 Flow Control Block Reservation Control Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FC_RSV_EN								FC_RSV_PMAP							
Type	RW								RW							
Reset	0								0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					FC_RSV_BLK_NUM				FC_RSV_QMAP							
Type					RW				RW							
Reset					0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	FC_RSV_EN	0: Disable 1: Enable queue block reservation
23:16	FC_RSV_PMAP	When FC_RSV_EN=1, Port map for queue block reservation Note: assume 8 port
11:8	FC_RSV_BLK_NUM	When FC_RSV_EN=1, Block size for queue block reservation Unit: 1 block
7:0	FC_RSV_QMAP	When FC_RSV_EN=1, Queue map for queue block reservation Unit: 1 block

00001FFC GIRLCR Global Ingress Rate Limit Control Register 00110118

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									IGC_FC_OFF_THD				IGC_FC_DROP_THD			
Type									RW				RW			
Reset									0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							IGC_MFRM_EX	IGC_IPG_OP	IGC_IPG_BYTE							

Type							RW	RW	RW							
Reset							0	1	0	0	0	1	1	0	0	0

Bit(s)	Name	Description
23:20	IGC_FC_OFF_THD	Ingress Rate Limit Pause-Off Threshold Pause-off frame is sent when the ingress token bucket is higher than pause-off threshold. Threshold = max_bucket_size >> igc_fc_off_thd
19:16	IGC_FC_DROP_THD	Ingress Rate Limit Drop Threshold If Port Flow Control and rate limit control is enabled, frame is drop when the ingress token bucket is less than drop threshold. Threshold = -(max_bucket_size >> igc_fc_drop_thd)
9	IGC_MFRM_EX	Ingress Rate Excludes Management Frames Management frames will be ignored by rate limit. (management frame type is set by ARL registers) 0: Include management frames 1: Exclude management frames
8	IGC_IPG_OP	Ingress Rate IPG Byte Addition or Subtraction Byte count should be added or subtracted on the rate calculation. 0: IPG byte is excluded 1: IPG byte is included
7:0	IGC_IPG_BYTE	Ingress Rate IPG Byte Count Byte count should be added while calculating the rate limit 8'h4: add 4 byte CRC (byte rate calculation) 8'h18: add 4 byte CRC + 8 byte Preamble + 12 byte IPG (line rate calculation)

5 Media Access Controller (MAC)

5.1 Introduction

The Ethernet MAC provides a solution for Ethernet applications operating at 10/100 Mbps using MII and 1000 Mbps using GMII interface, and it also support RGMII/revMII/SGMII in MT7531 port5. In addition to MAC layer function, it can also T/Rx some control frame to perform other network function, such as flow control, PFC, EEE, loop detection. Currently, WOL is not supported on 7531BE.

5.2 Features

5.2.1 MAC Layer function

It supports MAC layer functions in IEEE 802.3

- Support 10/100/1000 Mbps bit rates
- Support Half/Full duplex (1000Mbps Half Duplex Mode is not support)
- Automatic 32-bit CRC generation and checking
- Report packet status (good, CRC error, alignment, oversize, undersize, other MIBs information)
- Support collision detection and auto retransmission on collisions in half duplex mode (CSMA/CD protocol)
- PHY auto-polling, containing link status, speed mode, duplex mode, T/RX flow control ability, EEE ability
- Support packet length up to 15K for jumbo frames application

5.2.2 Interface translation

MT7531 supports GMII or MII in each MAC, and additionally supports RGMII/revMII/SGMII in port 5, users can select appropriate interface to fit their application.

5.2.3 Inter-Frame Gap Shrink

To resolve different frequency issue between two devices, user can enable inter-frame gap shrinkage function to shorten inter-frame gap from 96bits to 64bits. Besides, user can also select inter-frame gap random shrink, which will randomly shorten inter-frame gap to 64bits.

5.2.4 Flow Control

It support IEEE 802.3x flow control and automatic generation of control frames in full duplex mode. When flow-control is enabled and in full-duplex mode, if buffer space in MT7531 is lower than a programmable pause-on threshold, MAC will generate pause-on packet to stop link partner from sending packet. If buffer space is released and higher than another programmable pause-off

threshold, MAC will send pause-off packet to tell link partner to start sending packet. The flow control mechanism can prevent packet drop due to buffer space empty.

5.2.5 Energy Efficient Ethernet (EEE)

MT7531 MAC supports IEEE 802.3az Energy Efficient Ethernet (EEE) capability for full duplex mode, containing 100Base/1000Base EEE. User can enable EEE function for saving power. For example, if EEE function is enabled and there is no data to transmit for a while, MAC will send sleep signal to link partner and stop MAC clock for saving power, besides, MAC will periodically send refresh signal to maintain link status between devices. On the other hand, MAC can also detect EEE signal sent from remote link, and decide to enter or leave low power idle mode for saving power.

5.2.6 Priority Flow Control (PFC)

It support sending & receiving PFC (priority flow control) packet. If PFC function is enabled, SCH in MT7531 can pause input packet by priority instead of by input port. And if link partner support PFC, it can pause output packet by priority instead of by output port. MAC in MT7531 can generate PFC packet if SCH request and can parse PFC packet from link partner. User can use PFC function to pause some flow without stopping all packet from link partner.

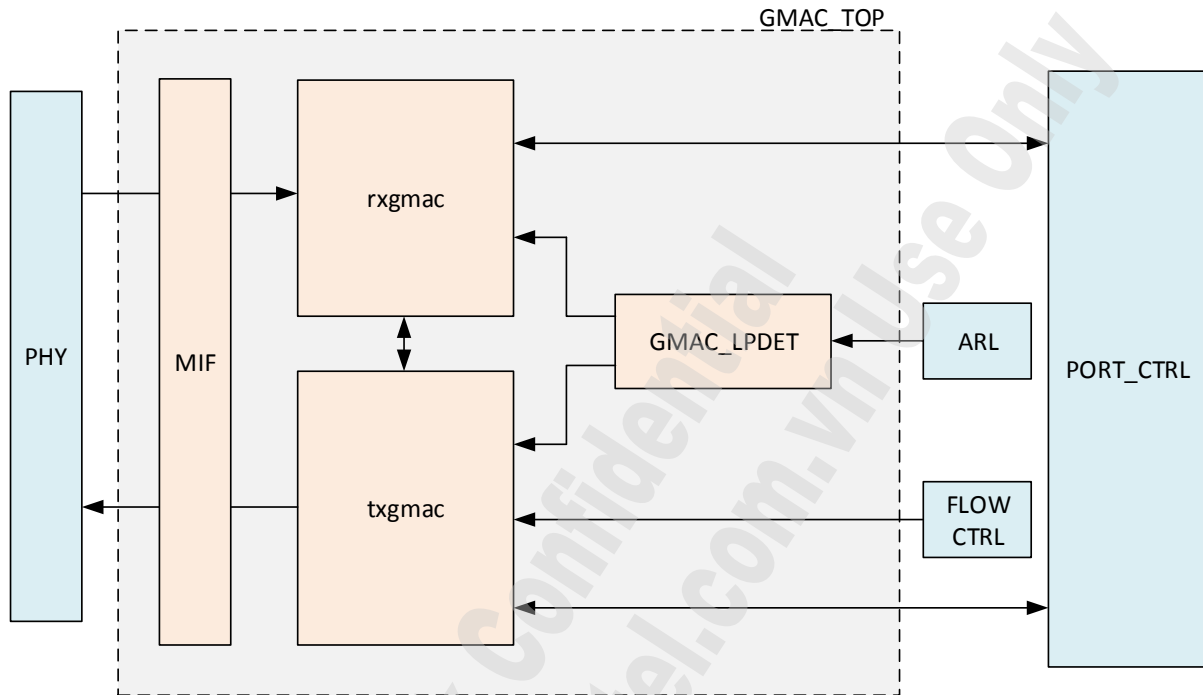
Besides, MT7531 support PFC auto-sync function, which can sync PFC ability automatically between different devices. If PFC auto-sync function is enabled, devices will automatically send PFC packet when linked-up, and will automatically enable PFC function if receiving any PFC packet from link partner.

5.2.7 Loop detection

MT7531 MAC support loop detection function, it can detect the loop in the network without running STP, which needs at least a processor with external memory.

If loop detection function is enabled, MAC will broadcast loop detection frames to each port when broadcast storm happens. If any port receives loop-detection frame just sent, it will detect loop condition occurrence at the port.

5.3 Block Diagram



MAC Function Blocks

RXMAC: MAC Receive Engine. The following tasks are performed.

- Check frame framing
- Remove frame preamble and frame SFD field
- Terminate pause frames
- Check frame length
- Calculate and verify CRC-32
- Write received frames in the RX FIFO
- Parsing pause frame and pause MAC TX
- Parsing PFC frame and tell SCH to pause corresponding priority
- Parsing WOL frame and send interrupt to system

TXMAC: MAC Transmit Engine. The following tasks are performed.

- Generate preamble and SFD field before frame transmission
- Generate pause frame if the memory manager reports congestion
- Generate PFC frame if the memory manager reports congestion
- Generate loop detection frame if broadcast storm is detected
- Calculate and append CRC-32 to the transmitted frame
- Send frame with correct IPG

MIF: multi-interface filter, it can translate RGMII/revMII into GMII

LPDET: It supports loop detect function in MAC

5.4 Register Definition

5.4.1 MAC Register

Module name: MAC Base address: (+0x0000)

Address	Name	Width	Register Function
00003000	<u>PMCR_P0</u>	32	PORT 0 MAC Control Register
00003004	<u>PMEEECR_P0</u>	32	PORT 0 MAC EEE Control Register
00003008	<u>PMSR_P0</u>	32	PORT 0 MAC Status Register
00003010	<u>PINT_EN_P0</u>	32	PORT 0 Interrupt Enable Register
00003014	<u>PINT_STS_P0</u>	32	PORT 0 Interrupt Status Register
00003018	<u>P0_DBG_CNT</u>	32	PORT 0 DEBUG COUNT
00003020	<u>P0_WOL</u>	32	PORT 0 WOL
00003024	<u>P0_PFC_STS</u>	32	PORT 0 PFC STATUS
00003030	<u>P0_PFC_RX_PSON_CNT_L</u>	32	Port 0 RX PFC pause on counter for low priority
00003034	<u>P0_PFC_RX_PSON_CNT_H</u>	32	Port 0 RX PFC pause on counter for high priority
00003038	<u>P0_PFC_RX_PSOFF_CNT_L</u>	32	Port 0 RX PFC pause off counter for low priority
0000303C	<u>P0_PFC_RX_PSOFF_CNT_H</u>	32	Port 0 RX PFC pause off counter for high priority
00003040	<u>P0_PFC_TX_PSON_CNT_L</u>	32	Port 0 TX PFC pause on counter for low priority
00003044	<u>P0_PFC_TX_PSON_CNT_H</u>	32	Port 0 TX PFC pause on counter for high priority
00003048	<u>P0_PFC_TX_PSOFF_CNT_L</u>	32	Port 0 TX PFC pause off counter for low priority
0000304C	<u>P0_PFC_TX_PSOFF_CNT_H</u>	32	Port 0 TX PFC pause off counter for high priority
000030B0	<u>PFC_CTRL</u>	32	PFC CONTROL REGISTER
000030B4	<u>PFC_AUTO_SYNC_DLY_SEL</u>	32	PFC AUTO SYNC DELAY SELECION
000030B8	<u>SGMII_2P5G_SPD_CTRL</u>	32	SGMII SPEED STATUS CONTROL REGISTER
000030C0	<u>LPDET_CTRL</u>	32	LOOP DETECTION CONTROL REGISTER
000030C8	<u>LPDET_SA_MSB</u>	32	LOOP DETECTION SA MSB
000030CC	<u>LPDET_SA_LSB</u>	32	LOOP DETECTION SA LSB
000030D0	<u>LPDET_RXSA_MSB</u>	32	LOOP DETECTION RX SA MSB
000030E0	<u>GMACCR</u>	32	Global MAC Control Register
000030E4	<u>SMACCR0</u>	32	System MAC Control Register 0
000030E8	<u>SMACCR1</u>	32	System MAC Control Register 1
000030F0	<u>CKGCR</u>	32	Clock Gating Control Register
000030F4	<u>GPINT_EN</u>	32	Global Port Interrupt Enable Register
000030F8	<u>GPINT_STS</u>	32	Global Port Interrupt Status Register
00003100	<u>PMCR_P1</u>	32	PORT 1 MAC Control Register
00003104	<u>PMEEECR_P1</u>	32	PORT 1 MAC EEE Control Register
00003108	<u>PMSR_P1</u>	32	PORT 1 MAC Status Register
00003110	<u>PINT_EN_P1</u>	32	PORT 1 Interrupt Enable Register
00003114	<u>PINT_STS_P1</u>	32	PORT 1 Interrupt Status Register
00003118	<u>P1_DBG_CNT</u>	32	PORT 1 DEBUG COUNT
00003120	<u>P1_WOL</u>	32	PORT 1 WOL
00003124	<u>P1_PFC_STS</u>	32	PORT 1 PFC STATUS
00003130	<u>P1_PFC_RX_PSON_CNT_L</u>	32	Port 1 RX PFC pause on counter for low priority

00003134	<u>P1_PFC_RX_PSON_CNT_H</u>	32	Port 1 RX PFC pause on counter for high priority
00003138	<u>P1_PFC_RX_PSOFF_CNT_L</u>	32	Port 1 RX PFC pause off counter for low priority
0000313C	<u>P1_PFC_RX_PSOFF_CNT_H</u>	32	Port 1 RX PFC pause off counter for high priority
00003140	<u>P1_PFC_TX_PSON_CNT_L</u>	32	Port 1 TX PFC pause on counter for low priority
00003144	<u>P1_PFC_TX_PSON_CNT_H</u>	32	Port 1 TX PFC pause on counter for high priority
00003148	<u>P1_PFC_TX_PSOFF_CNT_L</u>	32	Port 1 TX PFC pause off counter for low priority
0000314C	<u>P1_PFC_TX_PSOFF_CNT_H</u>	32	Port 1 TX PFC pause off counter for high priority
00003200	<u>PMCR_P2</u>	32	PORT 2 MAC Control Register
00003204	<u>PMEEECR_P2</u>	32	PORT 2 MAC EEE Control Register
00003208	<u>PMSR_P2</u>	32	PORT 2 MAC Status Register
00003210	<u>PINT_EN_P2</u>	32	PORT 2 Interrupt Enable Register
00003214	<u>PINT_STS_P2</u>	32	PORT 2 Interrupt Status Register
00003218	<u>P2_DBG_CNT</u>	32	PORT 2 DEBUG COUNT
00003220	<u>P2_WOL</u>	32	PORT 2 WOL
00003224	<u>P2_PFC_STS</u>	32	PORT 2 PFC STATUS
00003230	<u>P2_PFC_RX_PSON_CNT_L</u>	32	Port 2 RX PFC pause on counter for low priority
00003234	<u>P2_PFC_RX_PSON_CNT_H</u>	32	Port 2 RX PFC pause on counter for high priority
00003238	<u>P2_PFC_RX_PSOFF_CNT_L</u>	32	Port 2 RX PFC pause off counter for low priority
0000323C	<u>P2_PFC_RX_PSOFF_CNT_H</u>	32	Port 2 RX PFC pause off counter for high priority
00003240	<u>P2_PFC_TX_PSON_CNT_L</u>	32	Port 2 TX PFC pause on counter for low priority
00003244	<u>P2_PFC_TX_PSON_CNT_H</u>	32	Port 2 TX PFC pause on counter for high priority
00003248	<u>P2_PFC_TX_PSOFF_CNT_L</u>	32	Port 2 TX PFC pause off counter for low priority
0000324C	<u>P2_PFC_TX_PSOFF_CNT_H</u>	32	Port 2 TX PFC pause off counter for high priority
00003300	<u>PMCR_P3</u>	32	PORT 3 MAC Control Register
00003304	<u>PMEEECR_P3</u>	32	PORT 3 MAC EEE Control Register
00003308	<u>PMSR_P3</u>	32	PORT 3 MAC Status Register
00003310	<u>PINT_EN_P3</u>	32	PORT 3 Interrupt Enable Register
00003314	<u>PINT_STS_P3</u>	32	PORT 3 Interrupt Status Register
00003318	<u>P3_DBG_CNT</u>	32	PORT 3 DEBUG COUNT
00003320	<u>P3_WOL</u>	32	PORT 3 WOL
00003324	<u>P3_PFC_STS</u>	32	PORT 3 PFC STATUS
00003330	<u>P3_PFC_RX_PSON_CNT_L</u>	32	Port 3 RX PFC pause on counter for low priority
00003334	<u>P3_PFC_RX_PSON_CNT_H</u>	32	Port 3 RX PFC pause on counter for high priority
00003338	<u>P3_PFC_RX_PSOFF_CNT_L</u>	32	Port 3 RX PFC pause off counter for low priority
0000333C	<u>P3_PFC_RX_PSOFF_CNT_H</u>	32	Port 3 RX PFC pause off counter for high priority
00003340	<u>P3_PFC_TX_PSON_CNT_L</u>	32	Port 3 TX PFC pause on counter for low priority
00003344	<u>P3_PFC_TX_PSON_CNT_H</u>	32	Port 3 TX PFC pause on counter for high priority
00003348	<u>P3_PFC_TX_PSOFF_CNT_L</u>	32	Port 3 TX PFC pause off counter for low priority
0000334C	<u>P3_PFC_TX_PSOFF_CNT_H</u>	32	Port 3 TX PFC pause off counter for high priority
00003400	<u>PMCR_P4</u>	32	PORT 4 MAC Control Register
00003404	<u>PMEEECR_P4</u>	32	PORT 4 MAC EEE Control Register
00003408	<u>PMSR_P4</u>	32	PORT 4 MAC Status Register
00003410	<u>PINT_EN_P4</u>	32	PORT 4 Interrupt Enable Register
00003414	<u>PINT_STS_P4</u>	32	PORT 4 Interrupt Status Register
00003418	<u>P4_DBG_CNT</u>	32	PORT 4 DEBUG COUNT
00003420	<u>P4_WOL</u>	32	PORT 4 WOL
00003424	<u>P4_PFC_STS</u>	32	PORT 4 PFC STATUS
00003430	<u>P4_PFC_RX_PSON_CNT_L</u>	32	Port 4 RX PFC pause on counter for low priority
00003434	<u>P4_PFC_RX_PSON_CNT_H</u>	32	Port 4 RX PFC pause on counter for high priority
00003438	<u>P4_PFC_RX_PSOFF_CNT_L</u>	32	Port 4 RX PFC pause off counter for low priority

0000343C	<u>P4 PFC RX PSOFF CNT H</u>	32	Port 4 RX PFC pause off counter for high priority
00003440	<u>P4 PFC TX PSON CNT L</u>	32	Port 4 TX PFC pause on counter for low priority
00003444	<u>P4 PFC TX PSON CNT H</u>	32	Port 4 TX PFC pause on counter for high priority
00003448	<u>P4 PFC TX PSOFF CNT L</u>	32	Port 4 TX PFC pause off counter for low priority
0000344C	<u>P4 PFC TX PSOFF CNT H</u>	32	Port 4 TX PFC pause off counter for high priority
00003500	<u>PMCR P5</u>	32	PORT 5 MAC Control Register
00003504	<u>PMEEECR P5</u>	32	PORT 5 MAC EEE Control Register
00003508	<u>PMSR P5</u>	32	PORT 5 MAC Status Register
00003510	<u>PINT_EN P5</u>	32	PORT 5 Interrupt Enable Register
00003514	<u>PINT_STS P5</u>	32	PORT 5 Interrupt Status Register
00003518	<u>P5_DBG_CNT</u>	32	PORT 5 DEBUG COUNT
00003520	<u>P5_WOL</u>	32	PORT 5 WOL
00003524	<u>P5_PFC_STS</u>	32	PORT 5 PFC STATUS
00003530	<u>P5 PFC RX PSON CNT L</u>	32	Port 5 RX PFC pause on counter for low priority
00003534	<u>P5 PFC RX PSON CNT H</u>	32	Port 5 RX PFC pause on counter for high priority
00003538	<u>P5 PFC RX PSOFF CNT L</u>	32	Port 5 RX PFC pause off counter for low priority
0000353C	<u>P5 PFC RX PSOFF CNT H</u>	32	Port 5 RX PFC pause off counter for high priority
00003540	<u>P5 PFC TX PSON CNT L</u>	32	Port 5 TX PFC pause on counter for low priority
00003544	<u>P5 PFC TX PSON CNT H</u>	32	Port 5 TX PFC pause on counter for high priority
00003548	<u>P5 PFC TX PSOFF CNT L</u>	32	Port 5 TX PFC pause off counter for low priority
0000354C	<u>P5 PFC TX PSOFF CNT H</u>	32	Port 5 TX PFC pause off counter for high priority
00003600	<u>PMCR P6</u>	32	PORT 6 MAC Control Register
00003604	<u>PMEEECR P6</u>	32	PORT 6 MAC EEE Control Register
00003608	<u>PMSR P6</u>	32	PORT 6 MAC Status Register
00003610	<u>PINT_EN P6</u>	32	PORT 6 Interrupt Enable Register
00003614	<u>PINT_STS P6</u>	32	PORT 6 Interrupt Status Register
00003618	<u>P6_DBG_CNT</u>	32	PORT 6 DEBUG COUNT
00003620	<u>P6_WOL</u>	32	PORT 6 WOL
00003624	<u>P6_PFC_STS</u>	32	PORT 6 PFC STATUS
00003630	<u>P6 PFC RX PSON CNT L</u>	32	Port 6 RX PFC pause on counter for low priority
00003634	<u>P6 PFC RX PSON CNT H</u>	32	Port 6 RX PFC pause on counter for high priority
00003638	<u>P6 PFC RX PSOFF CNT L</u>	32	Port 6 RX PFC pause off counter for low priority
0000363C	<u>P6 PFC RX PSOFF CNT H</u>	32	Port 6 RX PFC pause off counter for high priority
00003640	<u>P6 PFC TX PSON CNT L</u>	32	Port 6 TX PFC pause on counter for low priority
00003644	<u>P6 PFC TX PSON CNT H</u>	32	Port 6 TX PFC pause on counter for high priority
00003648	<u>P6 PFC TX PSOFF CNT L</u>	32	Port 6 TX PFC pause off counter for low priority
0000364C	<u>P6 PFC TX PSOFF CNT H</u>	32	Port 6 TX PFC pause off counter for high priority

00003000	<u>PMCR_P0</u>			PORT 0 MAC Control Register												00056330		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		

Name	FORCE_MOD E_LNK_P0	FORCE_MODE _SPD_P0	FORCE_MODE _DPX_P0	FORCE_MODE _RX_FC_P0	FORCE_MODE _TX_FC_P0	FORCE_MODE _EEE100_P0	FORCE_MODE _EEE1G_P0							IPG_CFG_P0		EXT_PH Y_P0	MAC_ MODE_P0
Type	RW	RW	RW	RW	RW	RW	RW							RW		RW	RW
Reset	0	0	0	0	0	0	0							0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		MAC_T X_EN_P0	MAC_R X_EN_P0		MAC_P RE_P0		BKOFF EN_P0	BACKP R_EN_P0	FORCE _EEE1G_P0	FORCE _EEE100_P0	FORCE _RX_FC_P0	FORCE _TX_FC_P0	FORCE_SPD_P0		FORCE _DPX_P0	FORCE _LNK_P0	
Type		RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW	
Reset		1	1		0		1	1	0	0	1	1	0	0	0	0	

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P0	PORT 0 link status force Mode. 0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P0 register)
30	FORCE_MODE_SPD_P0	PORT 0 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P0 register)
29	FORCE_MODE_DPX_P0	PORT 0 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module) 1: Force mode is on. (Mac duplex mode is determined by force_dpx_P0 register)
28	FORCE_MODE_RX_FC_P0	PORT 0 RX FC force Mode. 0: Force mode is off.(Mac RX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P0 register)
27	FORCE_MODE_TX_FC_P0	PORT 0 TX FC force Mode. 0: Force mode is off.(Mac TX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P0 register)
26	FORCE_MODE_EEE100_P0	PORT 0 100M EEE force Mode. 0: Force mode is off.(Mac 100M EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P0 register)
25	FORCE_MODE_EEE1G_P0	PORT 0 1G EEE force Mode. 0: Force mode is off.(Mac 1G EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P0 register)
19:18	IPG_CFG_P0	PORT 0 Inter-Frame+ Gap Shrink 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P0	PORT 0 External PHY. Port 0 connects with external PHY.

Bit(s)	Name	Description
		0: PORT 0 DOES NOT connect with external PHY 1: PORT 0 connects with external PHY
16	MAC_MODE_P0	PORT 0 MAC Mode. PORT 0 operates in MAC mode 0: PORT 0 operates in PHY mode. 1: PORT 0 operates in MAC mode.
14	MAC_TX_EN_P0	Port 0 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P0	PORT 0 RX MAC Enable. (Note: This bit only has impact on MAC function, it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P0	TX short preamble mode 0: TX short preamble length is disabled 1: TX short preamble is enabled.
9	BKOFF_EN_P0	PORT 0 Backoff Enable 0: Disabled 1: Let the MAC of PORT 0 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P0	PORT 0 Backpressure Enable 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P0	PORT 0 Force LPI Mode For 1000Mbps. When (force_mode_P0 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 0. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P0	PORT 0 Force LPI Mode For 100Mbps. When (force_mode_P0 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 0. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P0	PORT 0 Force RX FC. When (force_mode_P0 = 1), this bit is used to control the RX FC ability of PORT 0. 0: Disabled 1: Let the MAC of PORT 0 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P0	PORT 0 Force TX FC. When (force_mode_P0 = 1), this bit is used to control the TX FC ability of PORT 0. 0: Disabled 1: Let the MAC of PORT 0 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P0	PORT 0 Force Speed [1:0]. When (force_mode_P0 = 1), these bits are used to control MAC speed of PORT 0. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P0	PORT 0 Force duplex. When (force_mode_P0 = 1), this bit is used to control MAC duplex of PORT 0. 0: Half Duplex 1: Full Duplex

Bit(s)	Name	Description
0	FORCE_LNK_P0	PORT 0 Force MAC Link Up. When (force_mode_P0 = 1), this bit is used to control link status of PORT 0. 0: Link Down 1: Link Up

00003004 PMEEECR_P0 PORT 0 MAC EEE Control Register 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P0								WAKEUP_TIME_100_P0							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P0															LPI_MODE_EN_P0
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P0	PORT 0 Wake Up Time for 1000Mbps LPI Mode. The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P0	PORT 0 Wake Up Time for 100Mbps LPI Mode. The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P0	PORT 0 LPI Threshold. When there is no packet to be transmitted, and the idle time is greater than P0_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P0	PORT 0 Enter LPI Mode. When there is no packet to be transmitted, and the idle time is greater than P0_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P0_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003008		PMSR_P0				PORT 0 MAC Status Register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name									EEE1G_STS_P0	EEE100_STS_P0	RX_FC_STS_P0	TX_FC_STS_P0	MAC_SPD_STS_P0		MAC_DPX_STS_P0	MAC_LNK_STS_P0	
Type									RO	RO	RO	RO	RO		RO	RO	
Reset									0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
7	EEE1G_STS_P0	PORT 0 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P0	PORT 0 LPI Status Mode For 100Mbps 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P0	PORT 0 RX XFC Status. Port 0 Rx flow control status. 0: Disabled 1: Let the MAC of PORT 0 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P0	PORT 0 TX XFC Status. PORT 0 TX flow control status. 0: Disabled 1: Let the MAC of PORT 0 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P0	PORT 0 Speed [1:0] Status. Current speed of PORT 0 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P0	PORT 0 duplex Status. Current duplex mode of PORT 0 after PHY links up. 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P0	Port 6 Link Up Status. Link up status of PORT 0. 0: Link Down 1: Link Up

00003010		<u>PINT_EN_P0</u>			PORT 0 Interrupt Enable Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003014		PINT STS_P0				PORT 0 Interrupt Status Register								00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RC	RC	RC	RC	RC	RC	RC	RC					RC	RC	RC	RC
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt 0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt 0: False 1: True
10	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt 0: False 1: True
9	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt 0: False 1: True
8	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt 0: False 1: True
3	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt 0: False 1: True
2	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt 0: False 1: True
1	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt 0: False 1: True
0	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt 0: False 1: True

Bit(s)	Name	Description

00003018 P0_DBG_CNT PORT 0 DEBUG COUNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_FIFO_URUN					RX_FIFO_OV		
Type									RO					RO		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.

00003020 P0_WOL PORT 0 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port0 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port0 Wake-up On Lan Interrupt Status
16	WOL_STS	Port0 Wake-up On Lan Status
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.

Bit(s)	Name	Description
3	SNP_PKT	Port0 Wake-up On Lan with snoopy packet 0: Disable 1: Enable
2	CRC_DIS	Port0 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port0 Wake-up On Lan Interrupt Enable 0: Disable 1: Enable
0	WOL_EN	Port0 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003024		P0_PFC_STS				PORT 0 PFC STATUS								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	TX_PFC_STS								RX_PFC_STS								
Type	RO								RO								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port0 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port0 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003030		P0_PFC_RX_PSON_CNT_L				Port 0 RX PFC pause on counter for low priority										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT								
Type	RC								RC								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT								
Type	RC								RC								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port0 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port0 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port0 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port0 priority 0

00003034 P0_PFC_RX_PSON_CNT_H Port 0 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port0 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port0 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port0 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port0 priority 4

00003038 P0_PFC_RX_PSOFF_CNT_L Port 0 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 0

0000303C P0_PFC_RX_PSOFF_CNT_H Port 0 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port0 priority 4

00003040 P0_PFC_TX_PSON_CNT_L Port 0 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port0 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port0 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port0 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port0 priority 0

00003044 P0_PFC_TX_PSON_CNT_H Port 0 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port0 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port0 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port0 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port0 priority 4

00003048 P0 PFC TX PSOFF CNT L Port 0 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 0

0000304C P0 PFC TX PSOFF CNT H Port 0 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port0 priority 4

000030B0 PFC_CTRL PFC CONTROL REGISTER 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name												PFC_A UTO_E N6	PFC_A UTO_E N5	PFC_A UTO_E N4	PFC_A UTO_E N3	PFC_A UTO_E N2
Type												RO	RO	RO	RO	RO
Reset												0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	PFC_A UTO_E N1	PFC_A UTO_E N0	PFC_SY NC_EN 6	PFC_SY NC_EN 5	PFC_SY NC_EN 4	PFC_SY NC_EN 3	PFC_SY NC_EN 2	PFC_SY NC_EN 1	PFC_SY NC_EN 0	PFC_EN 6	PFC_EN 5	PFC_EN 4	PFC_EN 3	PFC_EN 2	PFC_EN 1	PFC_EN N0
Type	RO	RO	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
20	PFC_AUTO_EN6	PFC auto enable status of user port 6. 0: Disabled 1: Enabled
19	PFC_AUTO_EN5	PFC auto enable status of user port 5. 0: Disabled 1: Enabled
18	PFC_AUTO_EN4	PFC auto enable status of user port 4. 0: Disabled 1: Enabled
17	PFC_AUTO_EN3	PFC auto enable status of user port 3. 0: Disabled 1: Enabled
16	PFC_AUTO_EN2	PFC auto enable status of user port 2. 0: Disabled 1: Enabled
15	PFC_AUTO_EN1	PFC auto enable status of user port 1. 0: Disabled 1: Enabled
14	PFC_AUTO_EN0	PFC auto enable status of user port 0. 0: Disabled 1: Enabled
13	PFC_SYNC_EN6	Enable the PFC auto-sync ability of user port 6. 0: Disable 1: Enable

Bit(s)	Name	Description
12	PFC_SYNC_EN5	Enable the PFC auto-sync ability of user port 5. 0: Disable 1: Enable
11	PFC_SYNC_EN4	Enable the PFC auto-sync ability of user port 4. 0: Disable 1: Enable
10	PFC_SYNC_EN3	Enable the PFC auto-sync ability of user port 3. 0: Disable 1: Enable
9	PFC_SYNC_EN2	Enable the PFC auto-sync ability of user port 2. 0: Disable 1: Enable
8	PFC_SYNC_EN1	Enable the PFC auto-sync ability of user port 1. 0: Disable 1: Enable
7	PFC_SYNC_EN0	Enable the PFC auto-sync ability of user port 0. 0: Disable 1: Enable
6	PFC_EN6	Enable the PFC ability of user port 6. 0: Disable 1: Enable
5	PFC_EN5	Enable the PFC ability of user port 5. 0: Disable 1: Enable
4	PFC_EN4	Enable the PFC ability of user port 4. 0: Disable 1: Enable
3	PFC_EN3	Enable the PFC ability of user port 3. 0: Disable 1: Enable
2	PFC_EN2	Enable the PFC ability of user port 2. 0: Disable 1: Enable
1	PFC_EN1	Enable the PFC ability of user port 1. 0: Disable 1: Enable
0	PFC_EN0	Enable the PFC ability of user port 0. 0: Disable 1: Enable

000030B4		PFC_AUTO_SYNC_DLY_SEL PFC AUTO SYNC DELAY SELECTION										00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			PFC_AUTO_SY NC_DLY_SEL6	PFC_AUTO_SY NC_DLY_SEL5	PFC_AUTO_SY NC_DLY_SEL4	PFC_AUTO_SY NC_DLY_SEL3	PFC_AUTO_SY NC_DLY_SEL2	PFC_AUTO_SY NC_DLY_SEL1	PFC_AUTO_SY NC_DLY_SEL0							

Type			RW		RW		RW		RW		RW		RW		RW	
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:12	PFC_AUTO_SYNC_DLY_SEL6	Select the delay of sending PFC auto sync packet of user port 6 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
11:10	PFC_AUTO_SYNC_DLY_SEL5	Select the delay of sending PFC auto sync packet of user port 5 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
9:8	PFC_AUTO_SYNC_DLY_SEL4	Select the delay of sending PFC auto sync packet of user port 4 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
7:6	PFC_AUTO_SYNC_DLY_SEL3	Select the delay of sending PFC auto sync packet of user port 3 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
5:4	PFC_AUTO_SYNC_DLY_SEL2	Select the delay of sending PFC auto sync packet of user port 2 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
3:2	PFC_AUTO_SYNC_DLY_SEL1	Select the delay of sending PFC auto sync packet of user port 1 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s
1:0	PFC_AUTO_SYNC_DLY_SEL0	Select the delay of sending PFC auto sync packet of user port 0 0: Delay 0s 1: Delay 0.5s 2: Delay 1s 3: Delay 2s

000030B8	SGMII 2P5G SPD_CTRL					SGMII SPEED STATUS CONTROL REGISTER											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name											P6_SGMII_2P5G_SPD_STS	P5_SGMII_2P5G_SPD_STS	FORCE_P6_SGMII_2P5G_SPD	FORCE_P5_SGMII_2P5G_SPD	FORCE_MODE_P6_SGMII_2P5G_SPD	FORCE_MODE_P5_SGMII_2P5G_SPD
Type											RO	RO	RW	RW	RW	RW
Reset											0	0	0	0	0	0

Bit(s)	Name	Description
5	P6_SGMII_2P5G_SPD_STS	Port 6 SGMII speed status. 0: SGMII is not running at 2.5G 1: SGMII is running at 2.5G
4	P5_SGMII_2P5G_SPD_STS	Port 5 SGMII speed status. 0: SGMII is not running at 2.5G 1: SGMII is running at 2.5G
3	FORCE_P6_SGMII_2P5G_SPD	Force port 6 SGMII speed status. 0: SGMII is not running at 2.5G 1: SGMII is running at 2.5G
2	FORCE_P5_SGMII_2P5G_SPD	Force port 5 SGMII speed status. 0: SGMII is not running at 2.5G 1: SGMII is running at 2.5G
1	FORCE_MODE_P6_SGMII_2P5G_SPD	Port 6 SGMII speed force Mode. 0: Force mode is off 1: Force mode is on
0	FORCE_MODE_P5_SGMII_2P5G_SPD	Port 5 SGMII speed force Mode. 0: Force mode is off 1: Force mode is on

000030C0 LPDET_CTRL LOOP DETECTION CONTROL REGISTER 00130000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		LPDET_EN6	LPDET_EN5	LPDET_EN4	LPDET_EN3	LPDET_EN2	LPDET_EN1	LPDET_EN0	LPDET_PERIOD_EN	LPDET_ALARM_EN	LPDET_PASS	LPDET_PERIOD	LPDET_LED_RATE	LPDET_THRESHOLD		
Type		RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0	0	0	1	0	0	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPDET_ST_LOP	LPDET_ST_BCS								LPDET_ALARM_6	LPDET_ALARM_5	LPDET_ALARM_4	LPDET_ALARM_3	LPDET_ALARM_2	LPDET_ALARM_1	LPDET_ALARM_0
Type	RO	RO								RO	RO	RO	RO	RO	RO	W1C
Reset	0	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
30	LPDET_EN6	Enable the loop detection ability of user port 6. 0: Disable 1: Enable
29	LPDET_EN5	Enable the loop detection ability of user port 5. 0: Disable 1: Enable
28	LPDET_EN4	Enable the loop detection ability of user port 4. 0: Disable 1: Enable
27	LPDET_EN3	Enable the loop detection ability of user port 3. 0: Disable 1: Enable
26	LPDET_EN2	Enable the loop detection ability of user port 2. 0: Disable 1: Enable
25	LPDET_EN1	Enable the loop detection ability of user port 1. 0: Disable 1: Enable
24	LPDET_EN0	Enable the loop detection ability of user port 0. 0: Disable 1: Enable
23	LPDET_PERIOD_EN	The loop detection frame is triggered by a periodical timer or by broadcast storm. 0: Broadcast mode 1: Periodical mode
22	LPDET_ALARM_EN	Enable 2 kHz alarm output and per-port LED when loop is detected. 0: Disable 1: Enable
21	LPDET_PASS	Loop detection frame is blocked or passed to packet memory. 0: Blocked 1: Pass
20	LPDET_PERIOD	Interval of transmitting loop detection frame in Periodical mode. 0: 125 us 1: 1000 ms
19	LPDET_LED_RATE	LED blinking rate of per port when loop is detected. 0: LED blinking at 2 Hz 1: LED blinking at 4 Hz
18:16	LPDET_THRESHOLD	Number of missed loop detection frame before 2 kHz alarm is reset
15	LPDET_ST_LOOP	The status of loop detection. In LOOP state, the loop detection frame is transmitted, and the loop detection frames are received. 0: Not in Loop state 1: Loop state
14	LPDET_ST_BCST	The status of loop detection. In BCST state, the loop detection frame is transmitted, but no loop detection frame is received. 0: Not in BCST state 1: BCST state
6	LPDET_ALARM6	The status of loop detected on port 6. This bit is cleared when LPDET_ALARM0 is written as 1. 0: Not detected 1: Detected
5	LPDET_ALARM5	The status of loop detected on port 5. This bit is cleared when LPDET_ALARM0 is written as 1. 0: Not detected 1: Detected

Bit(s)	Name	Description
4	LPDET_ALARM4	The status of loop detected on port 4. This bit is cleared when LPDET_ALARM0 is written as 1. 0: Not detected 1: Detected
3	LPDET_ALARM3	The status of loop detected on port 3. This bit is cleared when LPDET_ALARM0 is written as 1. 0: Not detected 1: Detected
2	LPDET_ALARM2	The status of loop detected on port 2. This bit is cleared when LPDET_ALARM0 is written as 1. 0: Not detected 1: Detected
1	LPDET_ALARM1	The status of loop detected on port 1. This bit is cleared when LPDET_ALARM0 is written as 1. 0: Not detected 1: Detected
0	LPDET_ALARM0	The status of loop detected on port 0. This bit is cleared when it is written as 1. 0: Not detected 1: Detected

000030C8		LPDET_SA_MSB				LOOP DETECTION SA_MSB								88740180			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	LPDET_TYPE																
Type	RW																
Reset	1	0	0	0	1	0	0	0	0	1	1	1	0	1	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	LPDET_SA_MSB																
Type	RW																
Reset	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31:16	LPDET_TYPE	Loop detection frame type
15:0	LPDET_SA_MSB	Bits [47:32] of loop detection frame SA

000030CC		LPDET_SA_LSB				LOOP DETECTION SA_LSB								C2000001			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	LPDET_SA_LSB																
Type	RW																
Reset	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	LPDET_SA_LSB															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	LPDET_SA_LSB	Bits [31:00] of loop detection frame SA

000030D0 LPDET_RXSA_MSB LOOP DETECTION RX SA MSB 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LPDET_RXPORT				LPDET_SRCPORT			
Type									RO				RO			
Reset									0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
23:20	LPDET_RXPORT	This is the 4-bit port number from which the loop detection frame was received.
19:16	LPDET_SRCPORT	This is the 4-bit source port number in the received loop detection frame.

000030E0 GMACCR Global MAC Control Register 00001E3F

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													TXCRC_EN	RXCRC_EN	PRMBL_LMT_EN	
Type													RW	RW	RW	
Reset													0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				MTCC_LMT								MAX_RX_JUMBO				MAX_RX_PKT_LEN
Type				RW								RW				RW
Reset				1	1	1	1				1	1	1	1	1	1

Bit(s)	Name	Description
19	TXCRC_EN	TX CRC Enable 0: TX CRC insertion is enabled. 1: TX CRC insertion is disabled.
18	RXCRC_EN	RX CRC Enable 0: RX CRC removal is enabled. 1: RX CRC removal is disabled.
17	PRMBL_LMT_EN	Preamble Limit Enable 0: RXMAC can recognize SFD anytime. 1: RXMAC will recognize SFD within 7 Preamble bits, if SFD (0xd5) shows up after 7 bits preamble; RXMAC will not recognize it and treat it as no SFD case.
12:9	MTCC_LMT	MTCC Limit. Maximum transmitted collision count limitation 0: Disable TX collision abort function, send packet until the packet is sent successfully. 15: Maximum transmitted collision count is up to 15.
5:2	MAX_RX_JUMBO	Maximum length of ingress jumbo frames 0: Reserved. 1: Reserved. 2: 2K Bytes. 3: 3K Bytes. 4: 4K Bytes. 5: 5K Bytes. 6: 6K Bytes. 7: 7K Bytes. 8: 8K Bytes. 9: 9K Bytes. 10: 10K Bytes. 11: 11K Bytes. 12: 12K Bytes. 13: 13K Bytes. 14: 14K Bytes. 15: 15K Bytes.
1:0	MAX_RX_PKT_LEN	Max Receive Packet Length. Maximum length of ingress packet including CRC which can be received by MAC 0: 1518 bytes for untagged frames; 1522 bytes for tagged frames. 1: 1536bytes 2: 1552 bytes 3: MAX_RX_JUMBO

000030E4	SMACCR0												System MAC Control Register 0				0017A501		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	SMACCR0																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1			

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR0															
Type	RW															
Reset	1	0	1	0	0	1	0	1	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
31:0	SMACCR0	System MAC Address, sys_mac [31:0]. The first 32-bit of system MAC address. It is unique and is specified for pause frame.

000030E8 **SMACCR1** System MAC Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SMACCR1															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SMACCR1	System MAC Address, sys_mac [47:32]. The second 16-bit of system MAC address. It is unique and is specified for pause frame.

000030F0 **CKGCR** Clock Gating Control Register 00001E03

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_TXIDLE_THD										CKG_T XIDLE	CKG_R XLPI			CKG_L NKDN_ PORT	CKG_L NKDN_ GLB
Type	RW										RW	RW			RW	RW
Reset	0	0	0	1	1	1	1	0			0	0			1	1

Bit(s)	Name	Description
15:8	LPI_TXIDLE_THD	When there is no packet to be transmitted, and the idle time is greater than LPI_TXIDLE_THD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
5	CKG_TXIDLE	Default: 30ms (unit: 1ms) 0: Keep the TX port clock ticking. 1: Stop the TX port clock ticking when the corresponding port has no traffic to send, and the idle time is greater than <LPI_TXIDLE_THD> ms.
4	CKG_RXLPI	0: Keep RX port clock ticking. 1: Stop the RX port clock ticking when the corresponding port enters the LPI mode, and the RX FIFO is empty.
1	CKG_LNKDN_PORT	Port clock gating: Clock of gmac, port_ctrl, sch 0: Keep the RX and TX port clock ticking. 1: Stop both RX and TX port clock ticking when the corresponding port enters the link-down status for 2 seconds.
0	CKG_LNKDN_GLB	Global clock gating: Clock of bmu, pb_ctrl, arl 0: Keep the global clock ticking. 1: Stop the global clock ticking when port0~port5 enter the link-down status for 2 seconds.

000030F4		GPINT_EN				Global Port Interrupt Enable Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name							WOL_INT_EN	LPDET_INT_EN		PC6_IN_T_EN	PC5_IN_T_EN	PC4_IN_T_EN	PC3_IN_T_EN	PC2_IN_T_EN	PC1_IN_T_EN	PC0_IN_T_EN		
Type							RW	RW		RW	RW	RW	RW	RW	RW	RW		
Reset							0	0		0	0	0	0	0	0	0		

Bit(s)	Name	Description
9	WOL_INT_EN	Enable interrupt of Wake-On-LAN. 0: Disable 1: Enable
8	LPDET_INT_EN	Enable interrupt when the loop is detected. 0: Disable 1: Enable
6	PC6_INT_EN	Port Controller 6 Interrupt Enable 0: Disable 1: Enable
5	PC5_INT_EN	Port Controller 5 Interrupt Enable 0: Disable 1: Enable
4	PC4_INT_EN	Port Controller 4 Interrupt Enable 0: Disable

Bit(s)	Name	Description
3	PC3_INT_EN	1: Enable Port Controller 3 Interrupt Enable 0: Disable
2	PC2_INT_EN	1: Enable Port Controller 2 Interrupt Enable 0: Disable
1	PC1_INT_EN	1: Enable Port Controller 1 Interrupt Enable 0: Disable
0	PC0_INT_EN	1: Enable Port Controller 0 Interrupt Enable 0: Disable

000030F8	GPINT_STS				Global Port Interrupt Status Register												00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name							WOL_INT	LPDET_INT		PC6_INT	PC5_INT	PC4_INT	PC3_INT	PC2_INT	PC1_INT	PC0_INT	
Type							W1C	W1C		W1C	W1C	W1C	W1C	W1C	W1C	W1C	
Reset							0	0		0	0	0	0	0	0	0	

Bit(s)	Name	Description
9	WOL_INT	Wake-On-LAN interrupt status. This bit is cleared when it is written as 1. 0: False 1: True
8	LPDET_INT	Loop detection interrupt status. This bit is cleared when it is written as 1. 0: False 1: True
6	PC6_INT	Port Controller 6 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True
5	PC5_INT	Port Controller 5 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True
4	PC4_INT	Port Controller 4 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True
3	PC3_INT	Port Controller 3 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True

Bit(s)	Name	Description
2	PC2_INT	Port Controller 2 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True
1	PC1_INT	Port Controller 1 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True
0	PC0_INT	Port Controller 0 Interrupt. This bit is cleared when it is written as 1. 0: False 1: True

00003100		PMCR_P1				PORT 1 MAC Control Register								00056330			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	FORCE_MOD_E_LNK_P1	FORCE_MODE_SPD_P1	FORCE_MODE_DPX_P1	FORCE_MODE_RX_FC_P1	FORCE_MODE_TX_FC_P1	FORCE_MODE_EEE10_P1	FORCE_MODE_EEE1G_P1						IPG_CFG_P1		EXT_PHY_P1	MAC_MODE_P1	
Type	RW	RW	RW	RW	RW	RW	RW						RW		RW	RW	
Reset	0	0	0	0	0	0	0						0	1	0	1	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name		MAC_TX_EN_P1	MAC_RX_EN_P1		MAC_PRE_P1		BKOFF_EN_P1	BACKPR_EN_P1	FORCE_EEE1G_P1	FORCE_EEE10_P1	FORCE_RX_FC_P1	FORCE_TX_FC_P1	FORCE_SPD_P1		FORCE_DPX_P1	FORCE_LNK_P1	
Type		RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW	
Reset		1	1		0		1	1	0	0	1	1	0	0	0	0	

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P1	PORT 1 link status force Mode. 0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P1 register)
30	FORCE_MODE_SPD_P1	PORT 1 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P1 register)
29	FORCE_MODE_DPX_P1	PORT 1 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module) 1: Force mode is on. (Mac duplex mode is determined by force_dpx_P1 register)
28	FORCE_MODE_RX_FC_P1	PORT 1 RX FC force Mode. 0: Force mode is off.(Mac RX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P1 register)
27	FORCE_MODE_TX_FC_P1	PORT 1 TX FC force Mode.

Bit(s)	Name	Description
26	FORCE_MODE_EEE100_P1	0: Force mode is off.(Mac TX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P1 register) PORT 1 100M EEE force Mode. 0: Force mode is off.(Mac 100M EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P1 register)
25	FORCE_MODE_EEE1G_P1	PORT 1 1G EEE force Mode. 0: Force mode is off.(Mac 1G EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P1 register)
19:18	IPG_CFG_P1	PORT 1 Inter-Frame+ Gap Shrink. 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P1	PORT 1 External PHY. Port 1 connects with external PHY. 0: PORT 1 DOES NOT connect with external PHY 1: PORT 1 connects with external PHY
16	MAC_MODE_P1	PORT 1 MAC Mode. PORT 1 operates in MAC mode 0: PORT 1 operates in PHY mode 1: PORT 1 operates in MAC mode
14	MAC_TX_EN_P1	Port 1 TX MAC Enable (Note: This bit only has impacts on the MAC function, it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P1	PORT 1 RX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P1	TX short preamble mode 0: The TX short preamble length is disabled. 1: The TX short preamble is enabled.
9	BKOFF_EN_P1	PORT 1 Backoff Enable 0: Disabled 1: Let the MAC of PORT 1 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P1	PORT 1 Backpressure Enable 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P1	PORT 1 Force LPI Mode For 1000Mbps. When (force_mode_P1 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 1. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P1	PORT 1 Force LPI Mode For 100Mbps. When (force_mode_P1 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 1. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P1	PORT 1 Force RX FC. When (force_mode_P1 = 1), this bit is used to control the RX FC ability of PORT 1.

Bit(s)	Name	Description
		0: Disabled
4	FORCE_TX_FC_P1	1: Let the MAC of PORT 1 accept a pause frame when operating in full-duplex mode. PORT 1 Force TX FC. When (force_mode_P1 = 1), this bit is used to control the TX FC ability of PORT 1.
		0: Disabled
3:2	FORCE_SPD_P1	1: Let the MAC of PORT 1 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. PORT 1 Force Speed [1:0]. When (force_mode_P1 = 1), these bits are used to control MAC speed of PORT 1.
		00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: reserved
1	FORCE_DPX_P1	PORT 1 Force duplex. When (force_mode_P1 = 1), this bit is used to control MAC duplex of PORT 1.
		0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P1	PORT 1 Force MAC Link Up. When (force_mode_P1 = 1), this bit is used to control link status of PORT 1.
		0: Link Down 1: Link Up

00003104		PMEEECR_P1				PORT 1 MAC EEE Control Register								111E01E0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WAKEUP_TIME_1000_P1								WAKEUP_TIME_100_P1								
Type	RW								RW								
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	LPI_THRESH_P1															LPI_MODE_EN_P1	
Type	RW															RW	
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0	

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P1	PORT 1 Wake Up Time for 1000Mbps LPI Mode. The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P1	PORT 1 Wake Up Time for 100Mbps LPI Mode.

Bit(s)	Name	Description
		The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.
15:4	LPI_THRESH_P1	Time unit: 1 micro second PORT 1 LPI Threshold.
0	LPI_MODE_EN_P1	When there is no packet to be transmitted, and the idle time is greater than P1_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. PORT 1 Enter LPI Mode.
		When there is no packet to be transmitted, and the idle time is greater than P1_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P1_LPI_THRESHOLD. 1: Let the system enter the LPI mode immediately and send EEE LPI frame to the link partner.

00003108	PMSR_P1								PORT 1 MAC Status Register								00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name										EEE1G_STS_P1	EEE100_STS_P1	RX_FC_STS_P1	TX_FC_STS_P1	MAC_SPD_STS_P1	MAC_DPX_STS_P1	MAC_LNK_STS_P1	
Type										RO	RO	RO	RO	RO	RO	RO	
Reset										0	0	0	0	0	0	0	

Bit(s)	Name	Description
7	EEE1G_STS_P1	PORT 1 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P1	PORT 1 LPI Status Mode For 100Mbps 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P1	PORT 1 RX XFC Status. PORT 1 Rx flow control status. 0: Disabled 1: Let the MAC of PORT 1 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P1	PORT 1 TX XFC Status. PORT 1 TX flow control status. 0: Disabled 1: Let the MAC of PORT 1 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P1	PORT 1 Speed [1:0] Status. Current speed of PORT 1 after PHY links up.

Bit(s)	Name	Description
		00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P1	PORT 1 duplex Status. Current duplex mode of PORT 1 after PHY links up. 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P1	Port 1 Link Up Status. Link up status of PORT 1. 0: Link Down 1: Link Up

00003110		PINT_EN_P1								PORT 1 Interrupt Enable Register								00000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																			
Type																			
Reset																			
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name		TX_TFF_UNDR_INT_EN	TX_MISVLAN_ERR_INT_EN	TX_MISPAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TO_INT_EN	RX_GPAGE_TOUT_INT_EN		
Type		RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW		
Reset		0	0	0	0	0	0	0	0					0	0	0	0		

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable

Bit(s)	Name	Description
		0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003114	PINT_STS_P1				PORT 1 Interrupt Status Register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TO_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TO_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt 0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt

Bit(s)	Name	Description
		0: False 1: True
10	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt 0: False 1: True
9	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt 0: False 1: True
8	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt 0: False 1: True
3	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt 0: False 1: True
2	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt 0: False 1: True
1	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt 0: False 1: True
0	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt 0: False 1: True

00003118	P1_DBG_CNT				PORT 1 DEBUG COUNT												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name									TX_FIFO_URUN					RX_FIFO_OV					
Type									RO					RO					
Reset									0	0	0	0		0	0	0			

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.

00003120 P1_WOL

PORT 1 WOL

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_INT_STS	WOL_STS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_PKT	CRC_DIS	WOL_INT_EN	WOL_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port1 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port1 Wake-up On Lan Interrupt Status
16	WOL_STS	Port1 Wake-up On Lan Status
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
3	SNP_PKT	Port1 Wake-up On Lan with snoop packet 0: Disable 1: Enable
2	CRC_DIS	Port1 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port1 Wake-up On Lan Interrupt Enable 0: Disable 1: Enable
0	WOL_EN	Port1 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003124	P1_PFC_STS				PORT 1 PFC STATUS												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name																				
Type																				
Reset																				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	TX_PFC_STS								RX_PFC_STS											
Type	RO								RO											
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port1 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port1 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003130 P1_PFC_RX_PSON_CNT_L Port 1 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port1 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port1 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port1 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port1 priority 0

00003134 P1_PFC_RX_PSON_CNT_H Port 1 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port1 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port1 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port1 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port1 priority 4

00003138 P1_PFC_RX_PSOFF_CNT_L Port 1 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 0

0000313C P1_PFC_RX_PSOFF_CNT_H Port 1 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port1 priority 4

00003140 P1_PFC_TX_PSON_CNT_L Port 1 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port1 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port1 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port1 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port1 priority 0

00003144 P1_PFC_TX_PSON_CNT_H Port 1 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port1 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port1 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port1 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port1 priority 4

00003148 P1_PFC_TX_PSOFF_CNT_L Port 1 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 0

0000314C P1 PFC TX PSOFF CNT H Port 1 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port1 priority 4

00003200 PMCR_P2 PORT 2 MAC Control Register 00056130

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_MODE_LNK_P2	FORCE_MODE_SPD_P2	FORCE_MODE_DPX_P2	FORCE_MODE_RX_FC_P2	FORCE_MODE_TX_FC_P2	FORCE_MODE_EEE10_P2	FORCE_MODE_EEE1G_P2						IPG_CFG_P2		EXT_PHY_P2	MAC_MODE_P2
Type	RW	RW	RW	RW	RW	RW	RW						RW		RW	RW
Reset	0	0	0	0	0	0	0						0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MAC_TX_EN_P2	MAC_RX_EN_P2		MAC_PRE_P2			BACKP_R_EN_P2	FORCE_EEE1G_P2	FORCE_EEE10_P2	FORCE_RX_FC_P2	FORCE_TX_FC_P2	FORCE_SPD_P2		FORCE_DPX_P2	FORCE_LNK_P2
Type		RW	RW		RW			RW	RW	RW	RW	RW	RW		RW	RW
Reset		1	1		0			1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P2	PORT 2 link status force Mode.

Bit(s)	Name	Description
		0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P2 register)
30	FORCE_MODE_SPD_P2	PORT 2 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P2 register)
29	FORCE_MODE_DPX_P2	PORT 2 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module) 1: Force mode is on. (Mac duplex mode is determined by force_dpx_P2 register)
28	FORCE_MODE_RX_FC_P2	PORT 2 RX FC force Mode. 0: Force mode is off.(Mac RX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P2 register)
27	FORCE_MODE_TX_FC_P2	PORT 2 TX FC force Mode. 0: Force mode is off.(Mac TX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P2 register)
26	FORCE_MODE_EEE100_P2	PORT 2 100M EEE force Mode. 0: Force mode is off.(Mac 100M EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P2 register)
25	FORCE_MODE_EEE1G_P2	PORT 2 1G EEE force Mode. 0: Force mode is off.(Mac 1G EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P2 register)
19:18	IPG_CFG_P2	PORT 2 Inter-Frame+ Gap Shrink 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P2	PORT 2 External PHY. Port 2 connects with external PHY. 0: PORT 2 DOES NOT connect with external PHY 1: PORT 2 connects with external PHY
16	MAC_MODE_P2	PORT 2 MAC Mode. PORT 2 operates in MAC mode 0: PORT 2 operates in PHY mode 1: PORT 2 operates in MAC mode
14	MAC_TX_EN_P2	Port 2 TX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P2	PORT 2 RX MAC Enable (Note: This bit only has impacts on MAC function, it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P2	TX short preamble mode 0: TX short preamble length is disabled 1: TX short preamble is enabled.
8	BACKPR_EN_P2	PORT 2 Backpressure Enable

Bit(s)	Name	Description
		0: Disabled
7	FORCE_EEE1G_P2	1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count. PORT 2 Force LPI Mode For 1000Mbps. When (force_mode_pn = 1), this bit is used to control the 1000Base-T EEE ability of PORT 2.
		0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P2	1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps. PORT 2 Force LPI Mode For 100Mbps. When (force_mode_pn = 1), this bit is used to control the 100Base-TX EEE ability of PORT 2.
		0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P2	1: Have the ability of entering EEE Low Power Idle mode for 100Mbps. PORT 2 Force RX FC. When (force_mode_P2 = 1), this bit is used to control the RX FC ability of PORT 2.
		0: Disabled.
4	FORCE_TX_FC_P2	1: Let the MAC of PORT 2 accept a pause frame when operating in full-duplex mode. PORT 2 Force TX FC. When (force_mode_P2 = 1), this bit is used to control the TX FC ability of PORT 2.
		0: Disabled.
3:2	FORCE_SPD_P2	1: Let the MAC of PORT 2 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. PORT 2 Force Speed [1:0]. When (force_mode_P2 = 1), these bits are used to control MAC speed of PORT 2.
		00: 10Mbps
		01: 100Mbps
		10: 1000Mbps
		11: Reserved
1	FORCE_DPX_P2	PORT 2 Force duplex. When (force_mode_P2 = 1), this bit is used to control the MAC duplex of PORT 2.
		0: Half Duplex
		1: Full Duplex
0	FORCE_LNK_P2	PORT 2 Force MAC Link Up. When (force_mode_P2 = 1), this bit is used to control the link status of PORT 2.
		0: Link Down
		1: Link Up

00003204	PMEEECR_P2								PORT 2 MAC EEE Control Register								111E01E0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WAKEUP_TIME_1000_P2								WAKEUP_TIME_100_P2								
Type	RW								RW								
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	LPI_THRESH_P2															LPI_MODE_EN_P2	
Type	RW															RW	
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0	

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P2	PORT 2 Wake Up Time for 1000Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P2	PORT 2 Wake Up Time for 100Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P2	PORT 2 LPI Threshold. When there is no packet to be transmitted, and the idle time is greater than P2_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P2	PORT 2 Enter LPI Mode. When there is no packet to be transmitted, and the idle time is greater than P2_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P2_LPI_THRESHOLD. 1: Let the system enter the LPI mode immediately and send EEE LPI frame to the link partner.

00003208				PMSR_P2				PORT 2 MAC Status Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name									EEE1G_STS_P2	EEE100_STS_P2	RX_FC_STS_P2	TX_FC_STS_P2	MAC_SPD_STS_P2		MAC_DPX_STS_P2	MAC_LNK_STS_P2			
Type									RO	RO	RO	RO	RO		RO	RO			
Reset									0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
7	EEE1G_STS_P2	PORT 2 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P2	PORT 2 LPI Status Mode For 100Mbps

Bit(s)	Name	Description
5	RX_FC_STS_P2	0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps PORT 2 RX XFC Status. Port 2 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 2 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P2	PORT 2 TX XFC Status PORT 2 TX flow control status 0: Disabled. 1: Let the MAC of PORT 2 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P2	PORT 2 Speed [1:0] Status Current speed of PORT 2 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P2	PORT 2 duplex Status Current duplex mode of PORT 2 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P2	Port 2 Link Up Status Link up status of PORT 2 0: Link Down 1: Link Up

00003210		PINT_EN_P2										PORT 2 Interrupt Enable Register					00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	TX_TFF_UNDR_INT_EN	TX_MIS_VLAN_ERR_INT_EN	TX_MIS_PAGE_ERR_INT_EN	TX_RP_PAGE_ERR_INT_EN	TX_RP_OUT_INT_EN	TX_GP_OUT_INT_EN	TX_RD_PB_INT_EN	TX_DE_Q_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOU_INT_EN	RX_WRPB_TOU_INT_EN	RX_GPAGE_OUT_INT_EN		
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0					0	0	0	0		

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable

Bit(s)	Name	Description
		0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003214	PINT_STS_P2				PORT 2 Interrupt Status Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt 0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt 0: False 1: True
10	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt 0: False 1: True
9	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt 0: False 1: True
8	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt 0: False 1: True
3	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt 0: False 1: True
2	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt 0: False 1: True
1	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt 0: False 1: True
0	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt 0: False 1: True

00003218		P2_DBG_CNT			PORT 2 DEBUG COUNT										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_FIFO_URUN					RX_FIFO_OV		
Type									RO					RO		

Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.

00003220	P2_WOL				PORT 2 WOL								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port2 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port2 Wake-up On Lan Interrupt Status
16	WOL_STS	Port2 Wake-up On Lan Status
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
3	SNP_PKT	Port2 Wake-up On Lan with snoopy packet 0: Disable 1: Enable
2	CRC_DIS	Port2 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port2 Wake-up On Lan Interrupt Enable 0: Disable 1: Enable
0	WOL_EN	Port2 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003224 P2_PFC_STS PORT 2 PFC STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port2 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port2 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003230 P2_PFC_RX_PSON_CNT_L Port 2 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port2 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port2 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port2 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port2 priority 0

00003234 P2_PFC_RX_PSON_CNT_H Port 2 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port2 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port2 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port2 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port2 priority 4

00003238 P2_PFC_RX_PSOFF_CNT_L Port 2 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 0

0000323C P2_PFC_RX_PSOFF_CNT_H Port 2 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 7

Bit(s)	Name	Description
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port2 priority 4

00003240 P2_PFC_TX_PSON_CNT_L Port 2 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port2 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port2 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port2 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port2 priority 0

00003244 P2_PFC_TX_PSON_CNT_H Port 2 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port2 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port2 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port2 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port2 priority 4

00003248 P2 PFC TX PSOFF CNT L Port 2 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 0

0000324C P2 PFC TX PSOFF CNT H Port 2 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port2 priority 4

00003300 PMCR_P3 PORT 3 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_MODE_E_LNK_P3	FORCE_MODE_SPD_P3	FORCE_MODE_DPX_P3	FORCE_MODE_RX_FC_P3	FORCE_MODE_TX_FC_P3	FORCE_MODE_EEE10_P3	FORCE_MODE_EEE1G_P3						IPG_CFG_P3		EXT_PHY_P3	MAC_MODE_P3
Type	RW	RW	RW	RW	RW	RW	RW						RW		RW	RW

Reset	0	0	0	0	0	0	0						0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MAC_TX_EN_P3	MAC_RX_EN_P3		MAC_PREAMBLE_P3		BKOFF_EN_P3	BACKP_R_EN_P3	FORCE_EEE1G_P3	FORCE_EEE100_P3	FORCE_RX_FC_P3	FORCE_TX_FC_P3	FORCE_SPD_P3		FORCE_DPX_P3	FORCE_LNK_P3
Type		RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset		1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P3	PORT 3 link status force Mode. 0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P3 register)
30	FORCE_MODE_SPD_P3	PORT 3 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P3 register)
29	FORCE_MODE_DPX_P3	PORT 3 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module) 1: Force mode is on. (Mac duplex mode is determined by force_dpx_P3 register)
28	FORCE_MODE_RX_FC_P3	PORT 3 RX FC force Mode. 0: Force mode is off.(Mac RX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P3 register)
27	FORCE_MODE_TX_FC_P3	PORT 3 TX FC force Mode. 0: Force mode is off.(Mac TX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P3 register)
26	FORCE_MODE_EEE100_P3	PORT 3 100M EEE force Mode. 0: Force mode is off.(Mac 100M EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P3 register)
25	FORCE_MODE_EEE1G_P3	PORT 3 1G EEE force Mode. 0: Force mode is off.(Mac 1G EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P3 register)
19:18	IPG_CFG_P3	PORT 3 Inter-Frame+ Gap Shrink 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P3	PORT 3 External PHY Port 3 connects with external PHY. 0: PORT 3 DOES NOT connect with external PHY 1: PORT 3 connects with external PHY

Bit(s)	Name	Description
16	MAC_MODE_P3	PORT 3 MAC Mode PORT 3 operates in MAC mode. 0: PORT 3 operates in PHY mode 1: PORT 3 operates in MAC mode
14	MAC_TX_EN_P3	Port 3 TX MAC Enable (Note: This bit only has impact on MAC function, it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled 1: TX MAC function is enabled
13	MAC_RX_EN_P3	PORT 3 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled 1: RX MAC function is enabled
11	MAC_PRE_P3	TX short preamble mode 0: TX short preamble length is disabled 1: TX short preamble is enabled.
9	BKOFF_EN_P3	PORT 3 Backoff Enable 0: Disabled 1: Let the MAC of PORT 3 to follow the back-off mechanism when collision happens.
8	BACKPR_EN_P3	PORT 3 Backpressure Enable 0: Disabled 1: Enable the back pressure mechanism when operating in half-duplex mode with low internal free memory page count .
7	FORCE_EEE1G_P3	PORT 3 Force LPI Mode For 1000Mbps When (force_mode_P3 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 3. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P3	PORT 3 Force LPI Mode For 100Mbps When (force_mode_P3 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 3. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P3	PORT 3 Force RX FC When (force_mode_P3 = 1), this bit is used to control the RX FC ability of PORT 3. 0: Disabled. 1: Let the MAC of PORT 3 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P3	PORT 3 Force TX FC When (force_mode_P3 = 1), this bit is used to control the TX FC ability of PORT 3. 0: Disabled. 1: Let the MAC of PORT 3 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P3	PORT 3 Force Speed [1:0]

Bit(s)	Name	Description
1	FORCE_DPX_P3	When (force_mode_P3 = 1), these bits are used to control the MAC speed of PORT 3. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved PORT 3 Force duplex.
0	FORCE_LNK_P3	When (force_mode_P3 = 1), this bit is used to control the MAC duplex of PORT 3. 0: Half Duplex 1: Full Duplex PORT 3 Force MAC Link Up
		When (force_mode_P3 = 1), this bit is used to control the link status of PORT 3. 0: Link Down 1: Link Up

00003304	PMEEECR_P3								PORT 3 MAC EEE Control Register					111E01E0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WAKEUP_TIME_1000_P3								WAKEUP_TIME_100_P3								
Type	RW								RW								
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	LPI_THRESH_P3															LPI_MODE_EN_P3	
Type	RW															RW	
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0	

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P3	PORT 3 Wake Up Time for 1000Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P3	PORT 3 Wake Up Time for 100Mbps LPI Mode. The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second

Bit(s)	Name	Description
15:4	LPI_THRESH_P3	PORT 3 LPI Threshold When there is no packet to be transmitted, and the idle time is greater than P3_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P3	PORT 3 Enter LPI Mode. When there is no packet to be transmitted, and the idle time is greater than P3_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P3_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003308	PMSR_P3				PORT 3 MAC Status Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name										EEE1G_STS_P3	EEE100_STS_P3	RX_FC_STS_P3	TX_FC_STS_P3	MAC_SPD_STS_P3		MAC_DPX_STS_P3	MAC_LNK_STS_P3	
Type										RO	RO	RO	RO	RO		RO	RO	
Reset										0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
7	EEE1G_STS_P3	PORT 3 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P3	PORT 3 LPI Status Mode For 100Mbps 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P3	PORT 3 RX XFC Status Port 3 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 3 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P3	PORT 3 TX XFC Status PORT 3 TX flow control status 0: Disabled. 1: Let the MAC of PORT 3 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.

Bit(s)	Name	Description
3:2	MAC_SPD_STS_P3	PORT 3 Speed [1:0] Status Current speed of PORT 3 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P3	PORT 3 duplex Status Current duplex mode of port 3 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P3	Port 3 Link Up Status Link up status of PORT 3 0: Link Down 1: Link Up

00003310	PINT_EN_P3				PORT 3 Interrupt Enable Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MIS_VLAN_ERR_INT_EN	TX_MIS_PAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPPB_TO_INT_EN	TX_RDPB_TO_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TO_INT_EN	RX_GPPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable

Bit(s)	Name	Description
		0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003314	PINT_STS_P3				PORT 3 Interrupt Status Register										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt

Bit(s)	Name	Description
		0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt 0: False 1: True
10	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt 0: False 1: True
9	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt 0: False 1: True
8	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt 0: False 1: True
3	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt 0: False 1: True
2	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt 0: False 1: True
1	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt 0: False 1: True
0	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt 0: False 1: True

00003318	P3_DBG_CNT				PORT 3 DEBUG COUNT												00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name									TX_FIFO_URUN					RX_FIFO_OV			
Type									RO					RO			
Reset									0	0	0	0		0	0	0	

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo
The field is increased when TX fifo underrun occurs.		

Bit(s)	Name	Description
2:0	RX_FIFO_OV	Overflow count of RX fifo

The field is increased when RX fifo overflow occurs.

00003320	P3_WOL				PORT 3 WOL								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port3 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port3 Wake-up On Lan Interrupt Status
16	WOL_STS	Port3 Wake-up On Lan Status
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
3	SNP_PKT	Port3 Wake-up On Lan with snoopy packet 0: Disable 1: Enable
2	CRC_DIS	Port3 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port3 Wake-up On Lan Interrupt Enable 0: Disable 1: Enable
0	WOL_EN	Port3 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003324				P3_PFC_STS				PORT 3 PFC STATUS								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			

Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port3 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port3 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003330 **P3_PFC_RX_PSON_CNT_L** Port 3 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port3 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port3 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port3 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port3 priority 0

00003334 **P3_PFC_RX_PSON_CNT_H** Port 3 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port3 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port3 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port3 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port3 priority 4

00003338 P3_PFC_RX_PSOFF_CNT_L Port 3 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 0

0000333C P3_PFC_RX_PSOFF_CNT_H Port 3 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port3 priority 4

00003340 P3_PFC_TX_PSON_CNT_L Port 3 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port3 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port3 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port3 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port3 priority 0

00003344 P3_PFC_TX_PSON_CNT_H Port 3 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port3 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port3 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port3 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port3 priority 4

00003348 P3_PFC_TX_PSOFF_CNT_L Port 3 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 0

0000334C P3 PFC TX PSOFF CNT H Port 3 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port3 priority 4

00003400 PMCR_P4 PORT 4 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_MOD_E_LNK_P4	FORCE_MODE_SPD_P4	FORCE_MODE_DPX_P4	FORCE_MODE_RX_FC_P4	FORCE_MODE_TX_FC_P4	FORCE_MODE_EEE10_P4	FORCE_MODE_EEE1G_P4						IPG_CFG_P4		EXT_PHY_P4	MAC_MODE_P4
Type	RW	RW	RW	RW	RW	RW	RW						RW		RW	RW
Reset	0	0	0	0	0	0	0						0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name		MAC_T X_EN_ P4	MAC_R X_EN_ P4		MAC_P RE_P4		BKOFF EN_P4	BACKP R_EN_ P4	FORCE EEE1G _P4	FORCE EEE10 _P4	FORCE RX_FC _P4	FORCE TX_FC _P4	FORCE_SPD_P4	FORCE DPX_ P4	FORCE LNK_ P4
Type		RW	RW		RW		RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset		1	1		0		1	1	0	0	1	1	0	0	0

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P4	PORT 4 link status force Mode. 0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P4 register)
30	FORCE_MODE_SPD_P4	PORT 4 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P4 register)
29	FORCE_MODE_DPX_P4	PORT 4 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module) 1: Force mode is on. (Mac duplex mode is determined by force_dpx_P4 register)
28	FORCE_MODE_RX_FC_P4	PORT 4 RX FC force Mode. 0: Force mode is off.(Mac RX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P4 register)
27	FORCE_MODE_TX_FC_P4	PORT 4 TX FC force Mode. 0: Force mode is off.(Mac TX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P4 register)
26	FORCE_MODE_EEE100_P4	PORT 4 100M EEE force Mode. 0: Force mode is off.(Mac 100M EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P4 register)
25	FORCE_MODE_EEE1G_P4	PORT 4 1G EEE force Mode. 0: Force mode is off.(Mac 1G EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P4 register)
19:18	IPG_CFG_P4	PORT 4 Inter-Frame+ Gap Shrink 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: shrink 64-bits IFG
17	EXT_PHY_P4	PORT 4 External PHY Port 4 connects with external PHY. 0: PORT 4 DOES NOT connect with external PHY 1: PORT 4 connects with external PHY
16	MAC_MODE_P4	PORT 4 MAC Mode PORT 4 operates in MAC mode.

Bit(s)	Name	Description
		0: PORT 4 operates in PHY mode 1: PORT 4 operates in MAC mode
14	MAC_TX_EN_P4	PORT 4 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P4	PORT 4 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P4	TX short preamble mode 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P4	PORT 4 Backoff Enable 0: Disabled 1: Let the MAC of PORT 4 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P4	PORT 4 Backpressure Enable 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P4	PORT 4 Force LPI Mode For 1000Mbps. When (force_mode_P4 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 4. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps.
6	FORCE_EEE100_P4	PORT 4 Force LPI Mode For 100Mbps. When (force_mode_P4 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 4. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps.
5	FORCE_RX_FC_P4	PORT 4 Force RX FC When (force_mode_P4 = 1), this bit is used to control the RX FC ability of PORT 4. 0: Disabled. 1: Let the MAC of PORT 4 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P4	PORT 4 Force TX FC When (force_mode_P4 = 1), this bit is used to control the TX FC ability of PORT 4. 0: Disabled. 1: Let the MAC of PORT 4 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P4	PORT 4 Force Speed [1:0] When (force_mode_P4 = 1), these bits are used to control MAC speed of PORT 4. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved

Bit(s)	Name	Description
1	FORCE_DPX_P4	PORT 4 Force duplex When (force_mode_P4 = 1), this bit is used to control MAC duplex of PORT 4. 0: Half Duplex 1: Full Duplex
0	FORCE_LNK_P4	PORT 4 Force MAC Link Up When (force_mode_P4 = 1), this bit is used to control link status of PORT 4. 0: Link Down 1: Link Up

00003404				PMEEECR_P4				PORT 4 MAC EEE Control Register								111E01E0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	WAKEUP_TIME_1000_P4								WAKEUP_TIME_100_P4										
Type	RW								RW										
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	LPI_THRESH_P4															LPI_MODE_EN_P4			
Type	RW															RW			
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0			

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P4	PORT 4 Wake Up Time for 1000Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P4	PORT 4 Wake Up Time for 100Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P4	PORT 4 LPI Threshold When there is no packet to be transmitted, and the idle time is greater than P4_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P4	PORT 4 Enter LPI Mode.

Bit(s)	Name	Description
		When there is no packet to be transmitted, and the idle time is greater than P4_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P4_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003408	PMSR_P4				PORT 4 MAC Status Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P4	EEE100_STS_P4	RX_FC_STS_P4	TX_FC_STS_P4	MAC_SPD_STS_P4		MAC_DPX_STS_P4	MAC_LNK_STS_P4
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P4	PORT 4 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P4	PORT 4 LPI Status Mode For 100Mbps 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P4	PORT 4 RX XFC Status Port 4 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 4 accept a pause frame when operating in full-duplex mode
4	TX_FC_STS_P4	PORT 4 TX XFC Status PORT 4 TX flow control status 0: Disabled. 1: Let the MAC of PORT 4 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P4	PORT 4 Speed [1:0] Status Current speed of PORT 4 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved

Bit(s)	Name	Description
1	MAC_DPX_STS_P4	PORT 4 duplex Status Current duplex mode of PORT 4 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P4	Port 4 Link Up Status Link up status of PORT 4 0: Link Down 1: Link Up

00003410		PINT_EN_P4				PORT 4 Interrupt Enable Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	TX_TFF_UNDR_INT_EN	TX_MIS_VLAN_ERR_INT_EN	TX_MIS_PAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN	
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW	
Reset	0	0	0	0	0	0	0	0					0	0	0	0	

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable 0: Disabled 1: Enabled
14	TX_MIS_VLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable 0: Disabled

Bit(s)	Name	Description
8	TX_DEQ_TOUT_INT_EN	1: Enabled TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled
3	RX_AFF_FULL_INT_EN	1: Enabled RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled
2	RX_ARL_TOUT_INT_EN	1: Enabled RX_CTRL ARL Timeout Interrupt Enable 0: Disabled
1	RX_WRPB_TOUT_INT_EN	1: Enabled RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled
0	RX_GPAGE_TOUT_INT_EN	1: Enabled RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003414	PINT_STS_P4				PORT 4 Interrupt Status Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TO_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TO_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt 0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt 0: False

Bit(s)	Name	Description
10	TX_GPAGE_TOUT_INT	1: True TX_CTRL Get Page Timeout Interrupt 0: False
9	TX_RDPB_TOUT_INT	1: True TX_CTRL RD_PB Timeout Interrupt 0: False
8	TX_DEQ_TOUT_INT	1: True TX_CTRL DEQ Timeout Interrupt 0: False
3	RX_AFF_FULL_INT	1: True RX_CTRL Agent FIFO Full Interrupt 0: False
2	RX_ARL_TOUT_INT	1: True RX_CTRL ARL Timeout Interrupt 0: False
1	RX_WRPB_TOUT_INT	1: True RX_CTRL WR_PB Timeout Interrupt 0: False
0	RX_GPAGE_TOUT_INT	1: True RX_CTRL Get Page Timeout Interrupt 0: False 1: True

00003418	P4_DBG_CNT				PORT 4 DEBUG COUNT										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_FIFO_URUN					RX_FIFO_OV		
Type									RO					RO		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo
2:0	RX_FIFO_OV	The field is increased when TX fifo underrun occurs. Overflow count of RX fifo
		The field is increased when RX fifo overflow occurs.

00003420 P4_WOL PORT 4 WOL 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_INT_STS	WOL_STS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_PKT	CRC_DIS	WOL_INT_EN	WOL_EN
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port4 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port4 Wake-up On Lan Interrupt Status
16	WOL_STS	Port4 Wake-up On Lan Status
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
3	SNP_PKT	Port4 Wake-up On Lan with snoopy packet 0: Disable 1: Enable
2	CRC_DIS	Port4 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port4 Wake-up On Lan Interrupt Enable 0: Disable 1: Enable
0	WOL_EN	Port4 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003424 P4_PFC_STS PORT 4 PFC STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port4 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port4 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003430 P4 PFC RX PSON_CNT_L Port 4 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port4 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port4 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port4 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port4 priority 0

00003434 P4 PFC RX PSON_CNT_H Port 4 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port4 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port4 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port4 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port4 priority 4

00003438 P4 PFC RX PSOFF_CNT_L Port 4 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 0

0000343C P4 PFC RX PSOFF_CNT_H Port 4 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port4 priority 4

00003440 P4 PFC TX PSOEN_CNT_L Port 4 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port4 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port4 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port4 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port4 priority 0

00003444 P4_PFC_TX_PSON_CNT_H Port 4 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port4 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port4 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port4 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port4 priority 4

00003448 P4_PFC_TX_PSOFF_CNT_L Port 4 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 0

0000344C P4 PFC TX PSOFF CNT H Port 4 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port4 priority 4

00003500 PMCR_P5 PORT 5 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_MODE_LNK_P5	FORCE_MODE_SPD_P5	FORCE_MODE_DPX_P5	FORCE_MODE_RX_FC_P5	FORCE_MODE_TX_FC_P5	FORCE_MODE_EEE10_P5	FORCE_MODE_EEE1G_P5						IPG_CFG_P5		EXT_PHY_P5	MAC_MODE_P5
Type	RW	RW	RW	RW	RW	RW	RW						RW		RW	RW
Reset	0	0	0	0	0	0	0						0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MAC_TX_EN_P5	MAC_RX_EN_P5		MAC_PRE_P5		BKOFF_EN_P5	BACKPR_EN_P5	FORCE_EEE1G_P5	FORCE_EEE10_P5	FORCE_RX_FC_P5	FORCE_TX_FC_P5	FORCE_SPD_P5		FORCE_DPX_P5	FORCE_LNK_P5
Type		RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset		1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P5	PORT 5 link status force Mode.

Bit(s)	Name	Description
		0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P5 register)
30	FORCE_MODE_SPD_P5	PORT 5 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P5 register)
29	FORCE_MODE_DPX_P5	PORT 5 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module) 1: Force mode is on. (Mac duplex mode is determined by force_dpx_P5 register)
28	FORCE_MODE_RX_FC_P5	PORT 5 RX FC force Mode. 0: Force mode is off.(Mac RX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P5 register)
27	FORCE_MODE_TX_FC_P5	PORT 5 TX FC force Mode. 0: Force mode is off.(Mac TX FC ability is determined by phy auto-polling module) 1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P5 register)
26	FORCE_MODE_EEE100_P5	PORT 5 100M EEE force Mode. 0: Force mode is off.(Mac 100M EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P5 register)
25	FORCE_MODE_EEE1G_P5	PORT 5 1G EEE force Mode. 0: Force mode is off.(Mac 1G EEE ability is determined by phy auto-polling module) 1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P5 register)
19:18	IPG_CFG_P5	PORT 5 Inter-Frame+ Gap Shrink 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P5	PORT 5 External PHY Port 5 connects with external PHY. 0: PORT 5 DOES NOT connect with external PHY. 1: PORT 5 connects with external PHY.
16	MAC_MODE_P5	PORT 5 MAC Mode PORT 5 operates in MAC mode. 0: PORT 5 operates in PHY mode. 1: PORT 5 operates in MAC mode.
14	MAC_TX_EN_P5	Port 5 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P5	PORT 5 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled. 1: RX MAC function is enabled.

Bit(s)	Name	Description
11	MAC_PRE_P5	TX short preamble mode 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P5	PORT 5 Backoff Enable 0: Disabled 1: Let the MAC of PORT 5 follow the back-off mechanism when collision happens.
8	BACKPR_EN_P5	PORT 5 Backpressure Enable 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex mode with low internal free memory page count.
7	FORCE_EEE1G_P5	PORT 5 Force LPI Mode For 1000Mbps When (force_mode_P5 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps
6	FORCE_EEE100_P5	PORT 5 Force LPI Mode For 100Mbps When (force_mode_P5 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 5. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps
5	FORCE_RX_FC_P5	PORT 5 Force RX FC When (force_mode_P5 = 1), this bit is used to control the RX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	FORCE_TX_FC_P5	PORT 5 Force TX FC When (force_mode_P5 = 1), this bit is used to control the TX FC ability of PORT 5. 0: Disabled. 1: Let the MAC of PORT 5 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	FORCE_SPD_P5	PORT 5 Force Speed [1:0] When (force_mode_P5 = 1), these bits are used to control MAC speed of PORT 5. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved
1	FORCE_DPX_P5	PORT 5 Force duplex When (force_mode_P5 = 1), this bit is used to control MAC duplex of PORT 5. 0: Half Duplex 1: Full Duplex

Bit(s)	Name	Description
0	FORCE_LNK_P5	PORT 5 Force MAC Link Up
		When (force_mode_P5 = 1), this bit is used to control link status of PORT 5.
		0: Link Down
		1: Link Up

00003504 **PMEEECR_P5** **PORT 5 MAC EEE Control Register** 111E01E0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WAKEUP_TIME_1000_P5								WAKEUP_TIME_100_P5							
Type	RW								RW							
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LPI_THRESH_P5															LPI_M ODE_E N_P5
Type	RW															RW
Reset	0	0	0	0	0	0	0	1	1	1	1	0				0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P5	PORT 5 Wake Up Time for 1000Mbps LPI Mode
		The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.
		Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P5	PORT 5 Wake Up Time for 100Mbps LPI Mode.
		The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup.
		Time unit: 1 micro second
15:4	LPI_THRESH_P5	PORT 5 LPI Threshold.
		When there is no packet to be transmitted, and the idle time is greater than P5_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P5	PORT 5 Enter LPI Mode
		When there is no packet to be transmitted, and the idle time is greater than P5_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
		0: LPI mode depends on the P5_LPI_THRESHOLD.
		1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

Bit(s)	Name	Description

00003508 PMSR_P5 PORT 5 MAC Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P5	EEE100_STS_P5	RX_FC_STS_P5	TX_FC_STS_P5	MAC_SPD_STS_P5	MAC_DPX_STS_P5	MAC_LNK_STS_P5	
Type									RO	RO	RO	RO	RO	RO	RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P5	PORT 5 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps 1: Capable of entering EEE Low Power Idle mode for 1000Mbps
6	EEE100_STS_P5	PORT 5 LPI Status Mode For 100Mbps 0: Not capable of entering EEE Low Power Idle mode for 100Mbps 1: Capable of entering EEE Low Power Idle mode for 100Mbps
5	RX_FC_STS_P5	PORT 5 RX XFC Status. Port 5 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 5 accept a pause frame when operating in full-duplex mode.
4	TX_FC_STS_P5	PORT 5 TX XFC Status PORT 5 TX flow control status 0: Disabled. 1: Let the MAC of PORT 5 to transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P5	PORT 5 Speed [1:0] Status Current speed of PORT 5 after PHY links up. 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P5	PORT 5 duplex Status Current duplex mode of port 5 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P5	Port 5 Link Up Status. Link up status of PORT 5. 0: Link Down 1: Link Up

Bit(s)	Name	Description

00003510 PINT_EN_P5 PORT 5 Interrupt Enable Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MIS_VLAN_ERR_INT_EN	TX_MIS_PAGE_ERR_INT_EN	TX_RPAGE_ERR_INT_EN	TX_RPAGE_TOUT_INT_EN	TX_GPAGE_TOUT_INT_EN	TX_RDPB_TOUT_INT_EN	TX_DEQ_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_ARL_TOUT_INT_EN	RX_WRPB_TOUT_INT_EN	RX_GPAGE_TOUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable 0: Disabled 1: Enabled
14	TX_MIS_VLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable 0: Disabled 1: Enabled

Bit(s)	Name	Description
1	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003514 **PINT_STS_P5** **PORT 5 Interrupt Status Register** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT	TX_MISVLAN_ERR_INT	TX_MISPAGE_ERR_INT	TX_RPAGE_ERR_INT	TX_RPAGE_TOUT_INT	TX_GPAGE_TOUT_INT	TX_RDPB_TOUT_INT	TX_DEQ_TOUT_INT					RX_AFF_FULL_INT	RX_ARL_TOUT_INT	RX_WRPB_TOUT_INT	RX_GPAGE_TOUT_INT
Type	RO	RO	RO	RO	RO	RO	RO	RO					RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt 0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt 0: False 1: True
10	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt 0: False 1: True
9	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt 0: False 1: True
8	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt 0: False 1: True

Bit(s)	Name	Description
3	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt 0: False 1: True
2	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt 0: False 1: True
1	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt 0: False 1: True
0	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt 0: False 1: True

00003518	P5_DBG_CNT				PORT 5 DEBUG COUNT								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_FIFO_URUN					RX_FIFO_OV		
Type									RO					RO		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo. The field is increased when TX fifo underrun occurs.
2:0	RX_FIFO_OV	Overflow count of RX fifo. The field is increased when RX fifo overflow occurs.

00003520	P5_WOL				PORT 5 WOL								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port5 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port5 Wake-up On Lan Interrupt Status
16	WOL_STS	Port5 Wake-up On Lan Status
If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.		
3	SNP_PKT	Port5 Wake-up On Lan with snoopy packet 0: Disable 1: Enable
2	CRC_DIS	Port5 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port5 Wake-up On Lan Interrupt Enable 0: Disable 1: Enable
0	WOL_EN	Port5 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003524	P5_PFC_STS				PORT 5 PFC STATUS								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port5 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port5 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003530	P5_PFC_RX_PSON_CNT_L					Port 5 RX PFC pause on counter for low priority										00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT											
Type	RC								RC											

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port5 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port5 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port5 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port5 priority 0

00003534 P5 PFC RX PSON_CNT_H Port 5 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port5 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port5 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port5 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port5 priority 4

00003538 P5 PFC RX PSOFF_CNT_L Port 5 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 0

0000353C P5_PFC_RX_PSOFF_CNT_H Port 5 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port5 priority 4

00003540 P5_PFC_TX_PSON_CNT_L Port 5 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port5 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port5 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port5 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port5 priority 0

Bit(s)	Name	Description

00003544 **P5_PFC_TX_PSON_CNT_H** Port 5 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port5 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port5 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port5 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port5 priority 4

00003548 **P5_PFC_TX_PSOFF_CNT_L** Port 5 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 0

0000354C **P5_PFC_TX_PSOFF_CNT_H** Port 5 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port5 priority 4

00003600 PMCR_P6 PORT 6 MAC Control Register 00056330

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	FORCE_MODE_LNK_P6	FORCE_MODE_SPD_P6	FORCE_MODE_DPX_P6	FORCE_MODE_RX_FC_P6	FORCE_MODE_TX_FC_P6	FORCE_MODE_EEE10_P6	FORCE_MODE_EEE1G_P6						IPG_CFG_P6		EXT_PHY_P6	MAC_MODE_P6
Type	RW	RW	RW	RW	RW	RW	RW						RW		RW	RW
Reset	0	0	0	0	0	0	0						0	1	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name		MAC_TX_EN_P6	MAC_RX_EN_P6		MAC_PRE_P6		BKOFF_EN_P6	BACKPR_EN_P6	FORCE_EEE1G_P6	FORCE_EEE10_P6	FORCE_RX_FC_P6	FORCE_TX_FC_P6	FORCE_SPD_P6		FORCE_DPX_P6	FORCE_LNK_P6
Type		RW	RW		RW		RW	RW	RW	RW	RW	RW	RW		RW	RW
Reset		1	1		0		1	1	0	0	1	1	0	0	0	0

Bit(s)	Name	Description
31	FORCE_MODE_LNK_P6	PORT 6 link status force Mode. 0: Force mode is off.(Mac link status is determined by phy auto-polling module) 1: Force mode is on. (Mac link status is determined by force_link_P6 register)
30	FORCE_MODE_SPD_P6	PORT 6 speed force Mode. 0: Force mode is off.(Mac speed is determined by phy auto-polling module) 1: Force mode is on. (Mac speed is determined by force_spd_P6 register)
29	FORCE_MODE_DPX_P6	PORT 6 duplex force Mode. 0: Force mode is off.(Mac duplex mode is determined by phy auto-polling module)

Bit(s)	Name	Description
28	FORCE_MODE_RX_FC_P6	1: Force mode is on. (Mac duplex mode is determined by force_dpx_P6 register) PORT 6 RX FC force Mode. 0: Force mode is off. (Mac RX FC ability is determined by phy auto-polling module)
27	FORCE_MODE_TX_FC_P6	1: Force mode is on. (Mac RX FC ability is determined by force_rx_fc_P6 register) PORT 6 TX FC force Mode. 0: Force mode is off. (Mac TX FC ability is determined by phy auto-polling module)
26	FORCE_MODE_EEE100_P6	1: Force mode is on. (Mac TX FC ability is determined by force_tx_fc_P6 register) PORT 6 100M EEE force Mode. 0: Force mode is off. (Mac 100M EEE ability is determined by phy auto-polling module)
25	FORCE_MODE_EEE1G_P6	1: Force mode is on. (Mac 100M EEE ability is determined by force_eee100_P6 register) PORT 6 1G EEE force Mode. 0: Force mode is off. (Mac 1G EEE ability is determined by phy auto-polling module)
19:18	IPG_CFG_P6	1: Force mode is on. (Mac 1G EEE ability is determined by force_eee1g_P6 register) PORT 6 Inter-Frame+ Gap Shrink 00: Normal 96-bits IFG 01: Transmit 96-bits IFG with short IFG in random behavior 10: Shrink 64-bits IFG
17	EXT_PHY_P6	PORT 6 External PHY. Port 6 connects with external PHY. 0: PORT 6 DOES NOT connect with external PHY. 1: PORT 6 connects with external PHY.
16	MAC_MODE_P6	PORT 6 MAC Mode. PORT 6 operates in MAC mode 0: PORT 6 operates in PHY mode. 1: PORT 6 operates in MAC mode.
14	MAC_TX_EN_P6	Port 6 TX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: TX MAC function is disabled. 1: TX MAC function is enabled.
13	MAC_RX_EN_P6	PORT 6 RX MAC Enable (Note: This bit only has impact on MAC function, and it has no impact on the link status or Queue manager.) 0: RX MAC function is disabled. 1: RX MAC function is enabled.
11	MAC_PRE_P6	TX short preamble mode 0: TX short preamble length is disabled. 1: TX short preamble is enabled.
9	BKOFF_EN_P6	PORT 6 Backoff Enable 0: Disabled 1: Let the MAC of PORT 6 to follow the back-off mechanism when collision happens.
8	BACKPR_EN_P6	PORT 6 Backpressure Enable 0: Disabled 1: Enable back pressure mechanism when operating in half-duplex with low internal free memory page count.
7	FORCE_EEE1G_P6	PORT 6 Force LPI Mode For 1000Mbps When (force_mode_P6 = 1), this bit is used to control the 1000Base-T EEE ability of PORT 6.

Bit(s)	Name	Description
6	FORCE_EEE100_P6	0: Do not have the ability of entering EEE Low Power Idle mode for 1000Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 1000Mbps. PORT 6 Force LPI Mode For 100Mbps
5	FORCE_RX_FC_P6	When (force_mode_P6 = 1), this bit is used to control the 100Base-TX EEE ability of PORT 6. 0: Do not have the ability of entering EEE Low Power Idle mode for 100Mbps. 1: Have the ability of entering EEE Low Power Idle mode for 100Mbps. PORT 6 Force RX FC. When (force_mode_P6 = 1), this bit is used to control the RX FC ability of PORT 6.
4	FORCE_TX_FC_P6	0: Disabled. 1: Let the MAC of PORT 6 accept a pause frame when operating in full-duplex mode. PORT 6 Force TX FC
3:2	FORCE_SPD_P6	When (force_mode_P6 = 1), this bit is used to control the TX FC ability of PORT 6. 0: Disabled. 1: Let the MAC of PORT 6 transmit a pause frame when operating in full-duplex mode with low internal free memory page count. PORT 6 Force Speed [1:0]
1	FORCE_DPX_P6	When (force_mode_P6 = 1), these bits are used to control MAC speed of PORT 6. 00: 10Mbps 01: 100Mbps 10: 1000Mbps 11: Reserved PORT 6 Force duplex
0	FORCE_LNK_P6	When (force_mode_P6 = 1), this bit is used to control MAC duplex of PORT 6. 0: Half Duplex 1: Full Duplex PORT 6 Force MAC Link Up
		When (force_mode_P6 = 1), this bit is used to control link status of PORT 6. 0: Link Down 1: Link Up

00003604	PMEEECR_P6								PORT 6 MAC EEE Control Register								111E01E0
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	WAKEUP_TIME_1000_P6								WAKEUP_TIME_100_P6								
Type	RW								RW								
Reset	0	0	0	1	0	0	0	1	0	0	0	1	1	1	1	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	LPI_THRESH_P6															LPI_MODE_EN_P6
Type	RW															RW
Reset	0	0	0	0	0	0	0	0	1	1	1	1	0			0

Bit(s)	Name	Description
31:24	WAKEUP_TIME_1000_P6	PORT 6 Wake Up Time for 1000Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
23:16	WAKEUP_TIME_100_P6	PORT 6 Wake Up Time for 100Mbps LPI Mode The minimum allowed time needed to wait for PHY to be fully functional, and TXMAC can transmit packet after wakeup. Time unit: 1 micro second
15:4	LPI_THRESH_P6	PORT 6 LPI Threshold When there is no packet to be transmitted, and the idle time is greater than P6_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner.
0	LPI_MODE_EN_P6	PORT 6 Enter LPI Mode When there is no packet to be transmitted, and the idle time is greater than P6_LPI_THRESHOLD, the TXMAC will automatically enter LPI (Low Power Idle) mode and send EEE LPI frame to the link partner. 0: LPI mode depends on the P6_LPI_THRESHOLD. 1: Let the system enter LPI mode immediately and send EEE LPI frame to the link partner.

00003608	PMSR_P6				PORT 6 MAC Status Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									EEE1G_STS_P6	EEE100STS_P6	RX_FC_STS_P6	TX_FC_STS_P6	MAC_SPD_STS_P6		MAC_DPX_STS_P6	MAC_LNK_STS_P6
Type									RO	RO	RO	RO	RO		RO	RO
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	EEE1G_STS_P6	PORT 6 LPI Mode Status For 1000Mbps 0: Not capable of entering EEE Low Power Idle mode for 1000Mbps. 1: Capable of entering EEE Low Power Idle mode for 1000Mbps.
6	EEE100_STS_P6	PORT 6 LPI Status Mode For 100Mbps 0: Not capable of entering EEE Low Power Idle mode for 100Mbps. 1: Capable of entering EEE Low Power Idle mode for 100Mbps.
5	RX_FC_STS_P6	PORT 6 RX XFC Status Port 6 Rx flow control status 0: Disabled. 1: Let the MAC of PORT 6 accept a pause frame when operating in full-duplex mode
4	TX_FC_STS_P6	PORT 6 TX XFC Status Port 6 TX flow control status 0: Disabled. 1: Let the MAC of PORT 6 transmit a pause frame when operating in full-duplex mode with low internal free memory page count.
3:2	MAC_SPD_STS_P6	PORT 6 Speed [1:0] Status Current speed of PORT 6 after PHY links up 00: 10 Mbps 01: 100 Mbps 10: 1000 Mbps 11: Reserved
1	MAC_DPX_STS_P6	PORT 6 duplex Status Current duplex mode of PORT 6 after PHY links up 0: Half Duplex 1: Full Duplex
0	MAC_LNK_STS_P6	Port 6 Link Up Status Link up status of PORT 6 0: Link Down 1: Link Up

00003610		PINT_EN_P6				PORT 6 Interrupt Enable Register								00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_TFF_UNDR_INT_EN	TX_MIS_VLAN_ERR_INT_EN	TX_MIS_PAGE_ERR_INT_EN	TX_RP_PAGE_ERR_INT_EN	TX_RP_PAGE_OUT_INT_EN	TX_GP_PAGE_OUT_INT_EN	TX_RD_PAGE_UT_INT_EN	TX_DE_PAGE_Q_TOUT_INT_EN					RX_AFF_FULL_INT_EN	RX_AR_L_TOUT_INT_EN	RX_WR_PB_TO_UT_INT_EN	RX_GP_PAGE_OUT_INT_EN
Type	RW	RW	RW	RW	RW	RW	RW	RW					RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0					0	0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT_EN	TXMAC TXFIFO Under run Interrupt Enable 0: Disabled 1: Enabled
14	TX_MISVLAN_ERR_INT_EN	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
13	TX_MISPAGE_ERR_INT_EN	TX_CTRL PKT INFO Page Mismatch Error Interrupt Enable 0: Disabled 1: Enabled
12	TX_RPAGE_ERR_INT_EN	TX_CTRL Release Page Count Error Interrupt Enable 0: Disabled 1: Enabled
11	TX_RPAGE_TOUT_INT_EN	TX_CTRL Release Page Timeout Interrupt Enable 0: Disabled 1: Enabled
10	TX_GPAGE_TOUT_INT_EN	TX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled
9	TX_RDPB_TOUT_INT_EN	TX_CTRL RD_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
8	TX_DEQ_TOUT_INT_EN	TX_CTRL DEQ Timeout Interrupt Enable 0: Disabled 1: Enabled
3	RX_AFF_FULL_INT_EN	RX_CTRL Agent FIFO Full Interrupt Enable 0: Disabled 1: Enabled
2	RX_ARL_TOUT_INT_EN	RX_CTRL ARL Timeout Interrupt Enable 0: Disabled 1: Enabled
1	RX_WRPB_TOUT_INT_EN	RX_CTRL WR_PB Timeout Interrupt Enable 0: Disabled 1: Enabled
0	RX_GPAGE_TOUT_INT_EN	RX_CTRL Get Page Timeout Interrupt Enable 0: Disabled 1: Enabled

00003614	PINT_STS_P6			PORT 6 Interrupt Status Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	TX_TFF_UNDR_INT	TX_MIS_VLAN_	TX_MIS_PAGE_	TX_RP_AGE_E RR_INT	TX_RP_AGE_T	TX_GP_AGE_T	TX_RD_P B_TO UT_INT	TX_DE_Q TOU T_INT					RX_AFF_FULL_INT	RX_AR_L TOU T_INT	RX_WR_P B_TO UT_INT	RX_GP_AGE_T	

		ERR_IN T	ERR_IN T		OUT_I NT	OUT_I NT										OUT_I NT
Type	RO	RO	RO	RO	RO	RO	RO	RO						RO	RO	RO
Reset	0	0	0	0	0	0	0	0						0	0	0

Bit(s)	Name	Description
15	TX_TFF_UNDR_INT	TXMAC TXFIFO Under run Interrupt 0: False 1: True
14	TX_MISVLAN_ERR_INT	TX_CTRL PKT INFO VLAN Mismatch Error Interrupt 0: False 1: True
13	TX_MISPAGE_ERR_INT	TX_CTRL PKT INFO Page Mismatch Error Interrupt 0: False 1: True
12	TX_RPAGE_ERR_INT	TX_CTRL Release Page Count Error Interrupt 0: False 1: True
11	TX_RPAGE_TOUT_INT	TX_CTRL Release Page Timeout Interrupt 0: False 1: True
10	TX_GPAGE_TOUT_INT	TX_CTRL Get Page Timeout Interrupt 0: False 1: True
9	TX_RDPB_TOUT_INT	TX_CTRL RD_PB Timeout Interrupt 0: False 1: True
8	TX_DEQ_TOUT_INT	TX_CTRL DEQ Timeout Interrupt 0: False 1: True
3	RX_AFF_FULL_INT	RX_CTRL Agent FIFO Full Interrupt 0: False 1: True
2	RX_ARL_TOUT_INT	RX_CTRL ARL Timeout Interrupt 0: False 1: True
1	RX_WRPB_TOUT_INT	RX_CTRL WR_PB Timeout Interrupt 0: False 1: True
0	RX_GPAGE_TOUT_INT	RX_CTRL Get Page Timeout Interrupt 0: False 1: True

00003618	P6_DBG_CNT				PORT 6 DEBUG COUNT												00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									TX_FIFO_URUN					RX_FIFO_OV		
Type									RO					RO		
Reset									0	0	0	0		0	0	0

Bit(s)	Name	Description
7:4	TX_FIFO_URUN	Underrun count of TX fifo.
2:0	RX_FIFO_OV	The field is increased when TX fifo underrun occurs. Overflow count of RX fifo
		The field is increased when RX fifo overflow occurs.

00003620	P6_WOL				PORT 6 WOL								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	WOL_DBG														WOL_I NT_STS	WOL_S TS
Type	RO														W1C	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													SNP_P KT	CRC_DI S	WOL_I NT_EN	WOL_E N
Type													RW	RW	RW	RW
Reset													0	0	0	0

Bit(s)	Name	Description
31:18	WOL_DBG	Port6 Wake-up On Lan Debug Signals
17	WOL_INT_STS	Port6 Wake-up On Lan Interrupt Status
16	WOL_STS	Port6 Wake-up On Lan Status
		If enable WOL_EN, this bit will change from 0 to 1 when GMAC RX state machine enter IDLE state. It indicates GMAC will drop all packets and detect magic packet.
3	SNP_PKT	Port6 Wake-up On Lan with snoopy packet 0: Disable 1: Enable
2	CRC_DIS	Port6 Wake-up On Lan with CRC Check Disable 0: CRC check enable 1: CRC check disable
1	WOL_INT_EN	Port6 Wake-up On Lan Interrupt Enable 0: Disable

Bit(s)	Name	Description
0	WOL_EN	1: Enable Port6 Wake-up On Lan Function Enable 0: Disable 1: Enable

00003624 P6_PFC_STS PORT 6 PFC STATUS 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PFC_STS								RX_PFC_STS							
Type	RO								RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:8	TX_PFC_STS	Port6 PFC TX pause on status of 8 priorities 1: pause on 0: pause off
7:0	RX_PFC_STS	Port6 PFC RX pause on status of 8 priorities 1: pause on 0: pause off

00003630 P6_PFC_RX_PSON_CNT_L Port 6 RX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSON_CNT								Q2_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSON_CNT								Q0_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSON_CNT	PFC RX pause on count for port6 priority 3
23:16	Q2_RX_PSON_CNT	PFC RX pause on count for port6 priority 2
15:8	Q1_RX_PSON_CNT	PFC RX pause on count for port6 priority 1
7:0	Q0_RX_PSON_CNT	PFC RX pause on count for port6 priority 0

00003634 P6 PFC RX PSON_CNT_H Port 6 RX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSON_CNT								Q6_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_RX_PSON_CNT								Q4_RX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSON_CNT	PFC RX pause on count for port6 priority 7
23:16	Q6_RX_PSON_CNT	PFC RX pause on count for port6 priority 6
15:8	Q5_RX_PSON_CNT	PFC RX pause on count for port6 priority 5
7:0	Q4_RX_PSON_CNT	PFC RX pause on count for port6 priority 4

00003638 P6 PFC RX PSOFF_CNT_L Port 6 RX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_RX_PSOFF_CNT								Q2_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_RX_PSOFF_CNT								Q0_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 3
23:16	Q2_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 2
15:8	Q1_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 1
7:0	Q0_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 0

0000363C P6 PFC RX PSOFF_CNT_H Port 6 RX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_RX_PSOFF_CNT								Q6_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	Q5_RX_PSOFF_CNT								Q4_RX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 7
23:16	Q6_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 6
15:8	Q5_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 5
7:0	Q4_RX_PSOFF_CNT	PFC RX pause off count for port6 priority 4

00003640 P6_PFC_TX_PSON_CNT_L Port 6 TX PFC pause on counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSON_CNT								Q2_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSON_CNT								Q0_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSON_CNT	PFC TX pause on count for port6 priority 3
23:16	Q2_TX_PSON_CNT	PFC TX pause on count for port6 priority 2
15:8	Q1_TX_PSON_CNT	PFC TX pause on count for port6 priority 1
7:0	Q0_TX_PSON_CNT	PFC TX pause on count for port6 priority 0

00003644 P6_PFC_TX_PSON_CNT_H Port 6 TX PFC pause on counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSON_CNT								Q6_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSON_CNT								Q4_TX_PSON_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSON_CNT	PFC TX pause on count for port6 priority 7
23:16	Q6_TX_PSON_CNT	PFC TX pause on count for port6 priority 6
15:8	Q5_TX_PSON_CNT	PFC TX pause on count for port6 priority 5
7:0	Q4_TX_PSON_CNT	PFC TX pause on count for port6 priority 4

00003648 P6_PFC_TX_PSOFF_CNT_L Port 6 TX PFC pause off counter for low priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q3_TX_PSOFF_CNT								Q2_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q1_TX_PSOFF_CNT								Q0_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q3_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 3
23:16	Q2_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 2
15:8	Q1_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 1
7:0	Q0_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 0

0000364C P6_PFC_TX_PSOFF_CNT_H Port 6 TX PFC pause off counter for high priority 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	Q7_TX_PSOFF_CNT								Q6_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	Q5_TX_PSOFF_CNT								Q4_TX_PSOFF_CNT							
Type	RC								RC							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:24	Q7_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 7
23:16	Q6_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 6
15:8	Q5_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 5
7:0	Q4_TX_PSOFF_CNT	PFC TX pause off count for port6 priority 4

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6 Management information base (MIB)

6.1 Introduction

MIB counter module supports Ethernet standard MIB counters of 7 Giga ports. Each Port MIB counter is implemented with 32x32 Single-port SRAM and registers. ARL MIB counters are implemented with registers.

MIB counter can be read/write accessed by three interfaces.

1. Port MAC MIB interface: When a packet is received or transmitted from a Port MAC, MIB will update the Enable signal which will be asserted with new information events to update Port MIB counter (SRAM).
2. ARL MIB interface: When ARL MIB events are received, ARL MIB counters will be increased by one.
3. P-Bus interface: The CPU host uses P-Bus to read/write Port MIB counters and ARLMIB counters.

The Port MAC module has higher priority for accessing Port MIB counters than P-Bus in order to update TX/RX MIB counters at 1000M line speed. Therefore, when Port MAC module and CPU module access Port MIB counters at the same time, the P-Bus access of CPU will be postponed till the Port MAC module updating process is completed. As for ARL MIB update module and CPU P-Bus module, the ARL update module has higher priority than the CPU P-Bus interface.

6.2 Features

- Support 7 Giga port Ethernet Switch MIB Counters
- Support MIB events for GMAC TX port
- Support MIB events for GMAC RX port
- Support MIB events for ARL module
- Support 32-bit P-Bus interface to read/write access MIB 32/64-bit registers
- Support 7 sets of 32x32 single port SRAM for MIB events memory

6.3 Block Diagram

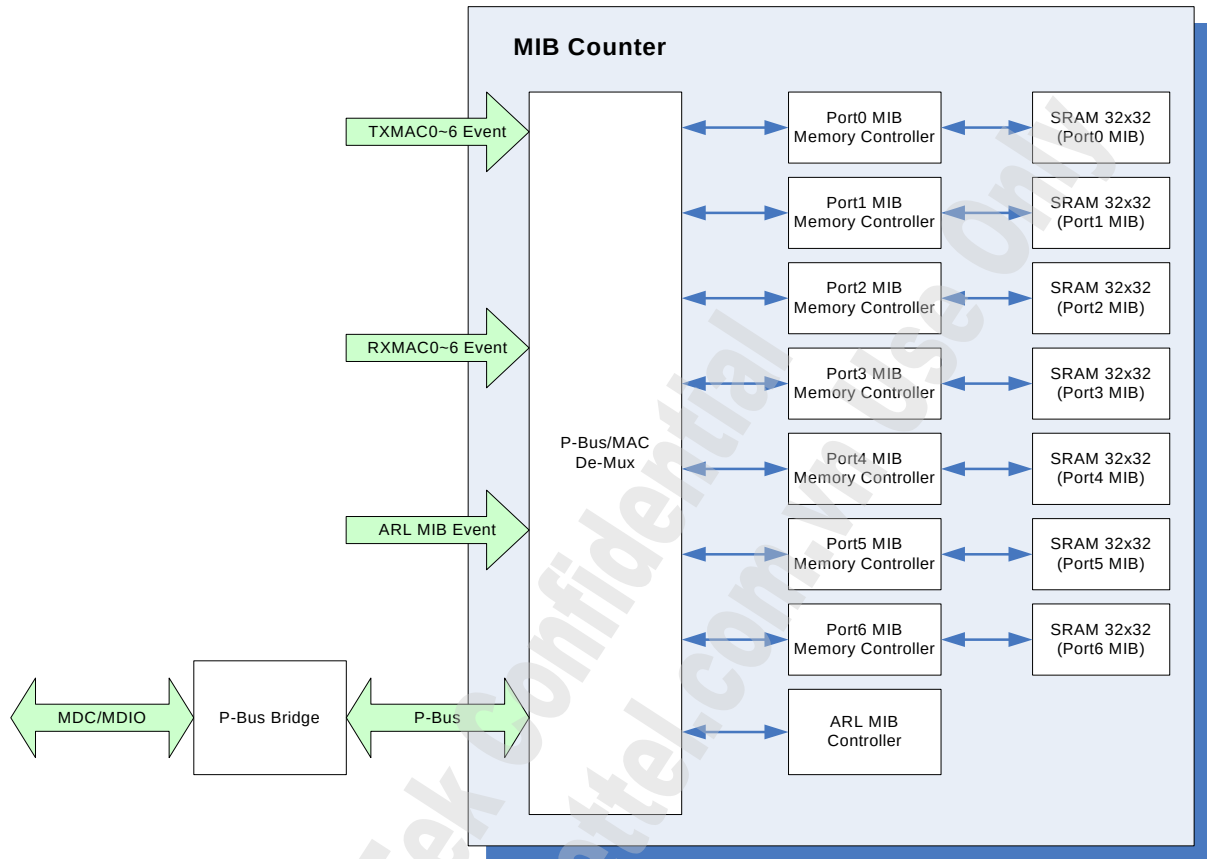


Figure 6-1. MIB block diagram

6.3.1 Overview of MIB Counters

The MIB module supports MIB counters for GMAC TX/RX ports and ARL module. All MIB counters are listed below.

Table 6-2. Overview of MIB Counters

Module	MIB Name	Bit width
Port 0 ~ 6	TX Drop Packet	32
	TX CRC Packet	32
	TX Unicast Packet	32
	TX Multicast Packet	32
	TX Broadcast Packet	32
	TX Collision Event Count	32
	TX Single Collision Event Count	32
	TX Multiple Collision Event Count	32
	TX Deferred Event Count	32

	TX Late Collision Event Count	32
	TX Excessive Collision Event Count	32
	TX Pause Packet	32
	TX Packet Length 64 bytes	32
	TX Packet Length 65 ~ 127 bytes	32
	TX Packet Length 128 ~ 255 bytes	32
	TX Packet Length 256 ~ 511 bytes	32
	TX Packet Length 512 ~ 1023 bytes	32
	TX/RX Packet Length 1024 ~ Max bytes	32
	TX Octets	64
	RX Drop Packet	32
	RX Filtering Packet	32
	RX Unicast Packet	32
	RX Multicast Packet	32
	RX Broadcast Packet	32
	RX Alignment Error Packet	32
	RX CRC Packet	32
	RX Undersize Packet	32
	RX Fragment Error Packet	32
	RX Oversize Packet	32
	RX Jabber Error Packet	32
	RX Pause Packet	32
	RX Packet Length 64 bytes	32
	RX Packet Length 65 ~ 127 bytes	32
	RX Packet Length 128 ~ 255 bytes	32
	RX Packet Length 256 ~ 511 bytes	32
	RX Packet Length 512 ~ 1023 bytes	32
	RX Packet Length 1024 ~ Max bytes	32
	RX Octets	64
	RX CTRL Drop Packet	32
	RX Ingress Drop Packet	32
	RX ARL Drop Packet	32
ARL	ARL Event 0	32
	ARL Event 1	32
	ARL Event 2	32
	ARL Event 3	32
	ARL Event 4	32
	ARL Event 5	32
	ARL Event 6	32
	ARL Event 7	32

6.4 Register Definition

Module name: MIB Base address: (+0x4000)

Address	Name	Width	Register Function
00004000	<u>TDPC_P0</u>	32	TX Drop Packet Counter of Port 0
00004004	<u>TCRC_P0</u>	32	TX CRC Packet Counter of Port 0
00004008	<u>TUPC_P0</u>	32	TX Unicast Packet Counter of Port 0
0000400C	<u>TMPC_P0</u>	32	TX Multicast Packet Counter of Port 0
00004010	<u>TBPC_P0</u>	32	TX Broadcast Packet Counter of Port 0
00004014	<u>TCEC_P0</u>	32	TX Collision Event Counter of Port 0
00004018	<u>TSCEC_P0</u>	32	TX Single Collision Event Counter of Port 0
0000401C	<u>TMCEC_P0</u>	32	TX Multiple Collision Event Counter of Port 0
00004020	<u>TDEC_P0</u>	32	TX Deferred Event Counter of Port 0
00004024	<u>TLCEC_P0</u>	32	TX Late Collision Event Counter of Port 0
00004028	<u>TXCEC_P0</u>	32	TX excessive Collision Event Counter of Port 0
0000402C	<u>TPPC_P0</u>	32	TX Pause Packet Counter of Port 0
00004030	<u>TL64PC_P0</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 0
00004034	<u>TL65PC_P0</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 0
00004038	<u>TL128PC_P0</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 0
0000403C	<u>TL256PC_P0</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 0
00004040	<u>TL512PC_P0</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 0
00004044	<u>TL1024PC_P0</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 0
00004048	<u>TOCL_P0</u>	32	TX Octet Counter Low double word of Port 0
0000404C	<u>TOCH_P0</u>	32	TX Octet Counter High double word of Port 0
00004060	<u>RDPC_P0</u>	32	RX Drop Packet Counter of Port 0
00004064	<u>RFPC_P0</u>	32	RX Filtering Packet Counter of Port 0
00004068	<u>RUPC_P0</u>	32	RX Unicast Packet Counter of Port 0
0000406C	<u>RMPC_P0</u>	32	RX Multicast Packet Counter of Port 0

00004070	<u>RBPC_P0</u>	32	RX Broadcast Packet Counter of Port 0
00004074	<u>RAEPC_P0</u>	32	RX Alignment Error Packet Counter of Port 0
00004078	<u>RCEPC_P0</u>	32	RX CRC(FCS) Error Packet Counter of Port 0
0000407C	<u>RUSPC_P0</u>	32	RX Undersize Packet Counter of Port 0
00004080	<u>RFEPC_P0</u>	32	RX Fragment Error Packet Counter of Port 0
00004084	<u>ROSPC_P0</u>	32	RX Oversize Packet Counter of Port 0
00004088	<u>RJEPC_P0</u>	32	RX Jabber Error Packet Counter of Port 0
0000408C	<u>RPPC_P0</u>	32	RX Pause Packet Counter of Port 0
00004090	<u>RL64PC_P0</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 0
00004094	<u>RL65PC_P0</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 0
00004098	<u>RL128PC_P0</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 0
0000409C	<u>RL256PC_P0</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 0
000040A0	<u>RL512PC_P0</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 0
000040A4	<u>RL1024PC_P0</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 0
000040A8	<u>ROCL_P0</u>	32	RX Octet Counter Low double word of Port 0
000040AC	<u>ROCH_P0</u>	32	Rx Octet Counter High double word of Port 0
000040B0	<u>RDPC_CTRL_P0</u>	32	RX CTRL Drop Packet Counter of Port 0
000040B4	<u>RDPC_ING_P0</u>	32	RX Ingress Drop Packet Counter of Port 0
000040B8	<u>RDPC_ARL_P0</u>	32	RX ARL Drop Packet Counter of Port 0
000040D0	<u>TMIB_HF_STS_P0</u>	32	TX Port MIB Counter Half Full Status of Port 0
000040D4	<u>RMIB_HF_STS_P0</u>	32	RX Port MIB Counter Half Full Status of Port 0
00004100	<u>TDPC_P1</u>	32	TX Drop Packet Counter of Port 1
00004104	<u>TCRC_P1</u>	32	TX CRC Packet Counter of Port 1
00004108	<u>TUPC_P1</u>	32	TX Unicast Packet Counter of Port 1
0000410C	<u>TMPC_P1</u>	32	TX Multicast Packet Counter of Port 1
00004110	<u>TBPC_P1</u>	32	TX Broadcast Packet Counter of Port 1
00004114	<u>TCEC_P1</u>	32	TX Collision Event Counter of Port 1

00004118	<u>TSCEC P1</u>	32	TX Single Collision Event Counter of Port 1
0000411C	<u>TMCEC P1</u>	32	TX Multiple Collision Event Counter of Port 1
00004120	<u>TDEC P1</u>	32	TX Deferred Event Counter of Port 1
00004124	<u>TLCEC P1</u>	32	TX Late Collision Event Counter of Port 1
00004128	<u>TXCEC P1</u>	32	TX excessive Collision Event Counter of Port 1
0000412C	<u>TPPC P1</u>	32	TX Pause Packet Counter of Port 1
00004130	<u>TL64PC P1</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 1
00004134	<u>TL65PC P1</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 1
00004138	<u>TL128PC P1</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 1
0000413C	<u>TL256PC P1</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 1
00004140	<u>TL512PC P1</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 1
00004144	<u>TL1024PC P1</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 1
00004148	<u>TOCL P1</u>	32	TX Octet Counter Low double word of Port 1
0000414C	<u>TOCH P1</u>	32	TX Octet Counter High double word of Port 1
00004160	<u>RDPC P1</u>	32	RX Drop Packet Counter of Port 1
00004164	<u>RFPC P1</u>	32	RX Filtering Packet Counter of Port 1
00004168	<u>RUPC P1</u>	32	RX Unicast Packet Counter of Port 1
0000416C	<u>RMPC P1</u>	32	RX Multicast Packet Counter of Port 1
00004170	<u>RBPC P1</u>	32	RX Broadcast Packet Counter of Port 1
00004174	<u>RAEPC P1</u>	32	RX Alignment Error Packet Counter of Port 1
00004178	<u>RCEPC P1</u>	32	RX CRC(FCS) Error Packet Counter of Port 1
0000417C	<u>RUSPC P1</u>	32	RX Undersize Packet Counter of Port 1
00004180	<u>RFEPC P1</u>	32	RX Fragment Error Packet Counter of Port 1
00004184	<u>ROSPC P1</u>	32	RX Oversize Packet Counter of Port 1
00004188	<u>RJEP C P1</u>	32	RX Jabber Error Packet Counter of Port 1
0000418C	<u>RPPC P1</u>	32	RX Pause Packet Counter of Port 1
00004190	<u>RL64PC P1</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 1

00004194	<u>RL65PC_P1</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 1
00004198	<u>RL128PC_P1</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 1
0000419C	<u>RL256PC_P1</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 1
000041A0	<u>RL512PC_P1</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 1
000041A4	<u>RL1024PC_P1</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 1
000041A8	<u>ROCL_P1</u>	32	RX Octet Counter Low double word of Port 1
000041AC	<u>ROCH_P1</u>	32	Rx Octet Counter High double word of Port 1
000041B0	<u>RDPC_CTRL_P1</u>	32	RX CTRL Drop Packet Counter of Port 1
000041B4	<u>RDPC_ING_P1</u>	32	RX Ingress Drop Packet Counter of Port 1
000041B8	<u>RDPC_ARL_P1</u>	32	RX ARL Drop Packet Counter of Port 1
000041D0	<u>TMIB_HF_STS_P1</u>	32	TX Port MIB Counter Half Full Status of Port 1
000041D4	<u>RMIB_HF_STS_P1</u>	32	RX Port MIB Counter Half Full Status of Port 1
00004200	<u>TDPC_P2</u>	32	TX Drop Packet Counter of Port 2
00004204	<u>TCRC_P2</u>	32	TX CRC Packet Counter of Port 2
00004208	<u>TUPC_P2</u>	32	TX Unicast Packet Counter of Port 2
0000420C	<u>TMPC_P2</u>	32	TX Multicast Packet Counter of Port 2
00004210	<u>TBPC_P2</u>	32	TX Broadcast Packet Counter of Port 2
00004214	<u>TCEC_P2</u>	32	TX Collision Event Counter of Port 2
00004218	<u>TSCEC_P2</u>	32	TX Single Collision Event Counter of Port 2
0000421C	<u>TMCEC_P2</u>	32	TX Multiple Collision Event Counter of Port 2
00004220	<u>TDEC_P2</u>	32	TX Deferred Event Counter of Port 2
00004224	<u>TLCEC_P2</u>	32	TX Late Collision Event Counter of Port 2
00004228	<u>TXCEC_P2</u>	32	TX excessive Collision Event Counter of Port 2
0000422C	<u>TPPC_P2</u>	32	TX Pause Packet Counter of Port 2
00004230	<u>TL64PC_P2</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 2
00004234	<u>TL65PC_P2</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 2
00004238	<u>TL128PC_P2</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 2

0000423C	<u>TL256PC_P2</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 2
00004240	<u>TL512PC_P2</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 2
00004244	<u>TL1024PC_P2</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 2
00004248	<u>TOCL_P2</u>	32	TX Octet Counter Low double word of Port 2
0000424C	<u>TOCH_P2</u>	32	TX Octet Counter High double word of Port 2
00004260	<u>RDPC_P2</u>	32	RX Drop Packet Counter of Port 2
00004264	<u>RFPC_P2</u>	32	RX Filtering Packet Counter of Port 2
00004268	<u>RUPC_P2</u>	32	RX Unicast Packet Counter of Port 2
0000426C	<u>RMPC_P2</u>	32	RX Multicast Packet Counter of Port 2
00004270	<u>RBPC_P2</u>	32	RX Broadcast Packet Counter of Port 2
00004274	<u>RAEPC_P2</u>	32	RX Alignment Error Packet Counter of Port 2
00004278	<u>RCEPC_P2</u>	32	RX CRC(FCS) Error Packet Counter of Port 2
0000427C	<u>RUSPC_P2</u>	32	RX Undersize Packet Counter of Port 2
00004280	<u>RFEP_C_P2</u>	32	RX Fragment Error Packet Counter of Port 2
00004284	<u>ROSPC_P2</u>	32	RX Oversize Packet Counter of Port 2
00004288	<u>RJEP_C_P2</u>	32	RX Jabber Error Packet Counter of Port 2
0000428C	<u>RPPC_P2</u>	32	RX Pause Packet Counter of Port 2
00004290	<u>RL64PC_P2</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 2
00004294	<u>RL65PC_P2</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 2
00004298	<u>RL128PC_P2</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 2
0000429C	<u>RL256PC_P2</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 2
000042A0	<u>RL512PC_P2</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 2
000042A4	<u>RL1024PC_P2</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 2
000042A8	<u>ROCL_P2</u>	32	RX Octet Counter Low double word of Port 2
000042AC	<u>ROCH_P2</u>	32	Rx Octet Counter High double word of Port 2
000042B0	<u>RDPC_CTRL_P2</u>	32	RX CTRL Drop Packet Counter of Port 2
000042B4	<u>RDPC_ING_P2</u>	32	RX Ingress Drop Packet Counter of Port 2

000042B8	<u>RDPC_ARL_P2</u>	32	RX ARL Drop Packet Counter of Port 2
000042D0	<u>TMIB_HF_STS_P2</u>	32	TX Port MIB Counter Half Full Status of Port 2
000042D4	<u>RMIB_HF_STS_P2</u>	32	RX Port MIB Counter Half Full Status of Port 2
00004300	<u>TDPC_P3</u>	32	TX Drop Packet Counter of Port 3
00004304	<u>TCRC_P3</u>	32	TX CRC Packet Counter of Port 3
00004308	<u>TUPC_P3</u>	32	TX Unicast Packet Counter of Port 3
0000430C	<u>TMPC_P3</u>	32	TX Multicast Packet Counter of Port 3
00004310	<u>TBPC_P3</u>	32	TX Broadcast Packet Counter of Port 3
00004314	<u>TCEC_P3</u>	32	TX Collision Event Counter of Port 3
00004318	<u>TSCEC_P3</u>	32	TX Single Collision Event Counter of Port 3
0000431C	<u>TMCEC_P3</u>	32	TX Multiple Collision Event Counter of Port 3
00004320	<u>TDEC_P3</u>	32	TX Deferred Event Counter of Port 3
00004324	<u>TLCEC_P3</u>	32	TX Late Collision Event Counter of Port 3
00004328	<u>TXCEC_P3</u>	32	TX excessive Collision Event Counter of Port 3
0000432C	<u>TPPC_P3</u>	32	TX Pause Packet Counter of Port 3
00004330	<u>TL64PC_P3</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 3
00004334	<u>TL65PC_P3</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 3
00004338	<u>TL128PC_P3</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 3
0000433C	<u>TL256PC_P3</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 3
00004340	<u>TL512PC_P3</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 3
00004344	<u>TL1024PC_P3</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 3
00004348	<u>TOCL_P3</u>	32	TX Octet Counter Low double word of Port 3
0000434C	<u>TOCH_P3</u>	32	TX Octet Counter High double word of Port 3
00004360	<u>RDPC_P3</u>	32	RX Drop Packet Counter of Port 3
00004364	<u>RFPC_P3</u>	32	RX Filtering Packet Counter of Port 3
00004368	<u>RUPC_P3</u>	32	RX Unicast Packet Counter of Port 3
0000436C	<u>RMPC_P3</u>	32	RX Multicast Packet Counter of Port 3

00004370	<u>RBPC_P3</u>	32	RX Broadcast Packet Counter of Port 3
00004374	<u>RAEPC_P3</u>	32	RX Alignment Error Packet Counter of Port 3
00004378	<u>RCEPC_P3</u>	32	RX CRC(FCS) Error Packet Counter of Port 3
0000437C	<u>RUSPC_P3</u>	32	RX Undersize Packet Counter of Port 3
00004380	<u>RFEPC_P3</u>	32	RX Fragment Error Packet Counter of Port 3
00004384	<u>ROSPC_P3</u>	32	RX Oversize Packet Counter of Port 3
00004388	<u>RJEP_C_P3</u>	32	RX Jabber Error Packet Counter of Port 3
0000438C	<u>RPPC_P3</u>	32	RX Pause Packet Counter of Port 3
00004390	<u>RL64PC_P3</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 3
00004394	<u>RL65PC_P3</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 3
00004398	<u>RL128PC_P3</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 3
0000439C	<u>RL256PC_P3</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 3
000043A0	<u>RL512PC_P3</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 3
000043A4	<u>RL1024PC_P3</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 3
000043A8	<u>ROCL_P3</u>	32	RX Octet Counter Low double word of Port 3
000043AC	<u>ROCH_P3</u>	32	Rx Octet Counter High double word of Port 3
000043B0	<u>RDPC_CTRL_P3</u>	32	RX CTRL Drop Packet Counter of Port 3
000043B4	<u>RDPC_ING_P3</u>	32	RX Ingress Drop Packet Counter of Port 3
000043B8	<u>RDPC_ARL_P3</u>	32	RX ARL Drop Packet Counter of Port 3
000043D0	<u>TMIB_HF_STS_P3</u>	32	TX Port MIB Counter Half Full Status of Port 3
000043D4	<u>RMIB_HF_STS_P3</u>	32	RX Port MIB Counter Half Full Status of Port 3
00004400	<u>TDPC_P4</u>	32	TX Drop Packet Counter of Port 4
00004404	<u>TCRC_P4</u>	32	TX CRC Packet Counter of Port 4
00004408	<u>TUPC_P4</u>	32	TX Unicast Packet Counter of Port 4
0000440C	<u>TMPC_P4</u>	32	TX Multicast Packet Counter of Port 4
00004410	<u>TBPC_P4</u>	32	TX Broadcast Packet Counter of Port 4
00004414	<u>TCEC_P4</u>	32	TX Collision Event Counter of Port 4

00004418	<u>TSCEC_P4</u>	32	TX Single Collision Event Counter of Port 4
0000441C	<u>TMCEC_P4</u>	32	TX Multiple Collision Event Counter of Port 4
00004420	<u>TDEC_P4</u>	32	TX Deferred Event Counter of Port 4
00004424	<u>TLCEC_P4</u>	32	TX Late Collision Event Counter of Port 4
00004428	<u>TXCEC_P4</u>	32	TX excessive Collision Event Counter of Port 4
0000442C	<u>TPPC_P4</u>	32	TX Pause Packet Counter of Port 4
00004430	<u>TL64PC_P4</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 4
00004434	<u>TL65PC_P4</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 4
00004438	<u>TL128PC_P4</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 4
0000443C	<u>TL256PC_P4</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 4
00004440	<u>TL512PC_P4</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 4
00004444	<u>TL1024PC_P4</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 4
00004448	<u>TOCL_P4</u>	32	TX Octet Counter Low double word of Port 4
0000444C	<u>TOCH_P4</u>	32	TX Octet Counter High double word of Port 4
00004460	<u>RDPC_P4</u>	32	RX Drop Packet Counter of Port 4
00004464	<u>RFPC_P4</u>	32	RX Filtering Packet Counter of Port 4
00004468	<u>RUPC_P4</u>	32	RX Unicast Packet Counter of Port 4
0000446C	<u>RMPC_P4</u>	32	RX Multicast Packet Counter of Port 4
00004470	<u>RBPC_P4</u>	32	RX Broadcast Packet Counter of Port 4
00004474	<u>RAEPC_P4</u>	32	RX Alignment Error Packet Counter of Port 4
00004478	<u>RCEPC_P4</u>	32	RX CRC(FCS) Error Packet Counter of Port 4
0000447C	<u>RUSPC_P4</u>	32	RX Undersize Packet Counter of Port 4
00004480	<u>RFEP_C_P4</u>	32	RX Fragment Error Packet Counter of Port 4
00004484	<u>ROSPC_P4</u>	32	RX Oversize Packet Counter of Port 4
00004488	<u>RJEP_C_P4</u>	32	RX Jabber Error Packet Counter of Port 4
0000448C	<u>RPPC_P4</u>	32	RX Pause Packet Counter of Port 4
00004490	<u>RL64PC_P4</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 4

00004494	<u>RL65PC_P4</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 4
00004498	<u>RL128PC_P4</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 4
0000449C	<u>RL256PC_P4</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 4
000044A0	<u>RL512PC_P4</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 4
000044A4	<u>RL1024PC_P4</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 4
000044A8	<u>ROCL_P4</u>	32	RX Octet Counter Low double word of Port 4
000044AC	<u>ROCH_P4</u>	32	Rx Octet Counter High double word of Port 4
000044B0	<u>RDPC_CTRL_P4</u>	32	RX CTRL Drop Packet Counter of Port 4
000044B4	<u>RDPC_ING_P4</u>	32	RX Ingress Drop Packet Counter of Port 4
000044B8	<u>RDPC_ARL_P4</u>	32	RX ARL Drop Packet Counter of Port 4
000044D0	<u>TMIB_HF_STS_P4</u>	32	TX Port MIB Counter Half Full Status of Port 4
000044D4	<u>RMIB_HF_STS_P4</u>	32	RX Port MIB Counter Half Full Status of Port 4
00004500	<u>TDPC_P5</u>	32	TX Drop Packet Counter of Port 5
00004504	<u>TCRC_P5</u>	32	TX CRC Packet Counter of Port 5
00004508	<u>TUPC_P5</u>	32	TX Unicast Packet Counter of Port 5
0000450C	<u>TMPC_P5</u>	32	TX Multicast Packet Counter of Port 5
00004510	<u>TBPC_P5</u>	32	TX Broadcast Packet Counter of Port 5
00004514	<u>TCEC_P5</u>	32	TX Collision Event Counter of Port 5
00004518	<u>TSCEC_P5</u>	32	TX Single Collision Event Counter of Port 5
0000451C	<u>TMCEC_P5</u>	32	TX Multiple Collision Event Counter of Port 5
00004520	<u>TDEC_P5</u>	32	TX Deferred Event Counter of Port 5
00004524	<u>TLCEC_P5</u>	32	TX Late Collision Event Counter of Port 5
00004528	<u>TXCEC_P5</u>	32	TX excessive Collision Event Counter of Port 5
0000452C	<u>TPPC_P5</u>	32	TX Pause Packet Counter of Port 5
00004530	<u>TL64PC_P5</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 5
00004534	<u>TL65PC_P5</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 5
00004538	<u>TL128PC_P5</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 5

0000453C	<u>TL256PC_P5</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 5
00004540	<u>TL512PC_P5</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 5
00004544	<u>TL1024PC_P5</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 5
00004548	<u>TOCL_P5</u>	32	TX Octet Counter Low double word of Port 5
0000454C	<u>TOCH_P5</u>	32	TX Octet Counter High double word of Port 5
00004560	<u>RDPC_P5</u>	32	RX Drop Packet Counter of Port 5
00004564	<u>RFPC_P5</u>	32	RX Filtering Packet Counter of Port 5
00004568	<u>RUPC_P5</u>	32	RX Unicast Packet Counter of Port 5
0000456C	<u>RMPC_P5</u>	32	RX Multicast Packet Counter of Port 5
00004570	<u>RBPC_P5</u>	32	RX Broadcast Packet Counter of Port 5
00004574	<u>RAEPC_P5</u>	32	RX Alignment Error Packet Counter of Port 5
00004578	<u>RCEPC_P5</u>	32	RX CRC(FCS) Error Packet Counter of Port 5
0000457C	<u>RUSPC_P5</u>	32	RX Undersize Packet Counter of Port 5
00004580	<u>RFEPC_P5</u>	32	RX Fragment Error Packet Counter of Port 5
00004584	<u>ROSPC_P5</u>	32	RX Oversize Packet Counter of Port 5
00004588	<u>RJEPC_P5</u>	32	RX Jabber Error Packet Counter of Port 5
0000458C	<u>RPPC_P5</u>	32	RX Pause Packet Counter of Port 5
00004590	<u>RL64PC_P5</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 5
00004594	<u>RL65PC_P5</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 5
00004598	<u>RL128PC_P5</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 5
0000459C	<u>RL256PC_P5</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 5
000045A0	<u>RL512PC_P5</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 5
000045A4	<u>RL1024PC_P5</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 5
000045A8	<u>ROCL_P5</u>	32	RX Octet Counter Low double word of Port 5
000045AC	<u>ROCH_P5</u>	32	Rx Octet Counter High double word of Port 5
000045B0	<u>RDPC_CTRL_P5</u>	32	RX CTRL Drop Packet Counter of Port 5
000045B4	<u>RDPC_ING_P5</u>	32	RX Ingress Drop Packet Counter of Port 5

000045B8	<u>RDPC_ARL_P5</u>	32	RX ARL Drop Packet Counter of Port 5
000045D0	<u>TMIB_HF_STS_P5</u>	32	TX Port MIB Counter Half Full Status of Port 5
000045D4	<u>RMIB_HF_STS_P5</u>	32	RX Port MIB Counter Half Full Status of Port 5
00004600	<u>TDPC_P6</u>	32	TX Drop Packet Counter of Port 6
00004604	<u>TCRC_P6</u>	32	TX CRC Packet Counter of Port 6
00004608	<u>TUPC_P6</u>	32	TX Unicast Packet Counter of Port 6
0000460C	<u>TMPC_P6</u>	32	TX Multicast Packet Counter of Port 6
00004610	<u>TBPC_P6</u>	32	TX Broadcast Packet Counter of Port 6
00004614	<u>TCEC_P6</u>	32	TX Collision Event Counter of Port 6
00004618	<u>TSCEC_P6</u>	32	TX Single Collision Event Counter of Port 6
0000461C	<u>TMCEC_P6</u>	32	TX Multiple Collision Event Counter of Port 6
00004620	<u>TDEC_P6</u>	32	TX Deferred Event Counter of Port 6
00004624	<u>TLCEC_P6</u>	32	TX Late Collision Event Counter of Port 6
00004628	<u>TXCEC_P6</u>	32	TX excessive Collision Event Counter of Port 6
0000462C	<u>TPPC_P6</u>	32	TX Pause Packet Counter of Port 6
00004630	<u>TL64PC_P6</u>	32	TX packet Length in 64-byte slot Packet Counter of Port 6
00004634	<u>TL65PC_P6</u>	32	TX packet Length in 65-byte slot Packet Counter of Port 6
00004638	<u>TL128PC_P6</u>	32	TX packet Length in 128-byte slot Packet Counter of Port 6
0000463C	<u>TL256PC_P6</u>	32	TX packet Length in 256-byte slot Packet Counter of Port 6
00004640	<u>TL512PC_P6</u>	32	TX packet Length in 512-byte slot Packet Counter of Port 6
00004644	<u>TL1024PC_P6</u>	32	TX packet Length in 1024-byte slot Packet Counter of Port 6
00004648	<u>TOCL_P6</u>	32	TX Octet Counter Low double word of Port 6
0000464C	<u>TOCH_P6</u>	32	TX Octet Counter High double word of Port 6
00004660	<u>RDPC_P6</u>	32	RX Drop Packet Counter of Port 6
00004664	<u>RFPC_P6</u>	32	RX Filtering Packet Counter of Port 6
00004668	<u>RUPC_P6</u>	32	RX Unicast Packet Counter of Port 6
0000466C	<u>RMPC_P6</u>	32	RX Multicast Packet Counter of Port 6

00004670	<u>RBPC_P6</u>	32	RX Broadcast Packet Counter of Port 6
00004674	<u>RAEPC_P6</u>	32	RX Alignment Error Packet Counter of Port 6
00004678	<u>RCEPC_P6</u>	32	RX CRC(FCS) Error Packet Counter of Port 6
0000467C	<u>RUSPC_P6</u>	32	RX Undersize Packet Counter of Port 6
00004680	<u>RFEPC_P6</u>	32	RX Fragment Error Packet Counter of Port 6
00004684	<u>ROSPC_P6</u>	32	RX Oversize Packet Counter of Port 6
00004688	<u>RJEPC_P6</u>	32	RX Jabber Error Packet Counter of Port 6
0000468C	<u>RPPC_P6</u>	32	RX Pause Packet Counter of Port 6
00004690	<u>RL64PC_P6</u>	32	RX packet Length in 64-byte slot Packet Counter of Port 6
00004694	<u>RL65PC_P6</u>	32	RX packet Length in 65-byte slot Packet Counter of Port 6
00004698	<u>RL128PC_P6</u>	32	RX packet Length in 128-byte slot Packet Counter of Port 6
0000469C	<u>RL256PC_P6</u>	32	RX packet Length in 256-byte slot Packet Counter of Port 6
000046A0	<u>RL512PC_P6</u>	32	RX packet Length in 512-byte slot Packet Counter of Port 6
000046A4	<u>RL1024PC_P6</u>	32	RX packet Length in 1024-byte slot Packet Counter of Port 6
000046A8	<u>ROCL_P6</u>	32	RX Octet Counter Low double word of Port 6
000046AC	<u>ROCH_P6</u>	32	Rx Octet Counter High double word of Port 6
000046B0	<u>RDPC_CTRL_P6</u>	32	RX CTRL Drop Packet Counter of Port 6
000046B4	<u>RDPC_ING_P6</u>	32	RX Ingress Drop Packet Counter of Port 6
000046B8	<u>RDPC_ARL_P6</u>	32	RX ARL Drop Packet Counter of Port 6
000046D0	<u>TMIB_HF_STS_P6</u>	32	TX Port MIB Counter Half Full Status of Port 6
000046D4	<u>RMIB_HF_STS_P6</u>	32	RX Port MIB Counter Half Full Status of Port 6
00004F00	<u>AE0CNT</u>	32	ACL Event 0 Counter
00004F04	<u>AE1CNT</u>	32	ACL Event 1 Counter
00004F08	<u>AE2CNT</u>	32	ACL Event 2 Counter
00004F0C	<u>AE3CNT</u>	32	ACL Event 3 Counter
00004F10	<u>AE4CNT</u>	32	ACL Event 4 Counter
00004F14	<u>AE5CNT</u>	32	ACL Event 5 Counter

00004F18	<u>AE6CNT</u>	32	ACL Event 6 Counter
00004F1C	<u>AE7CNT</u>	32	ACL Event 7 Counter
00004FE0	<u>MIBCCR</u>	32	MIB Counter Control
00004FE4	<u>AECCR</u>	32	ARL Event Counter Control
00004FE8	<u>AEMIB_HF_STS</u>	32	ARL Event MIB Counter Half Full Status
00004FF0	<u>MIBHF_INT_EN</u>	32	Port/ARL MIB Counter Half Full Interrupt Enable
00004FF4	<u>MIBHF_INT_STS</u>	32	Port/ARL MIB Counter Half Full Interrupt Status

00004000 TDPC_P0 TX Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event when the frame output should be dropped due to the late collision or excessive collision

00004004 TCRC_P0 TX CRC Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004008 TUPC_P0 TX Unicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.

0000400C TMPC_P0 TX Multicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004010 TBPC_P0 TX Broadcast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

00004014 TCEC_P0 TX Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	The total number of collision events occurrence during frame transmission

Bit(s)	Name	Description

00004018 **TSCEC_P0** TX Single Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_SCOL_CNT The number of frames transmitted without any error following a single collision

0000401C **TMCEC_P0** TX Multiple Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_MCOL_CNT The number of frames transmitted without any error following multiple collisions

00004020 TDEC_P0 TX Deferred Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted

00004024 TLCEC_P0 TX Late Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004028 TXCEC_P0 TX excessive Collision Event Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000402C TPPC_P0 TX Pause Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correct transmitted MAC flow-control frame

00004030 TL64PC_P0 TX packet Length in 64-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004034 TL65PC_P0 TX packet Length in 65-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004038 TL128PC_P0 TX packet Length in 128-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000403C TL256PC_P0 TX packet Length in 256-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.

00004040 TL512PC_P0 TX packet Length in 512-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

00004044 TL1024PC_P0 TX packet Length in 1024-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

00004048 TOCL_P0 TX Octet Counter Low double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000404C TOCH_P0 TX Octet Counter High double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004060 RDPC_P0 RX Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004064 RFPC_P0 RX Filtering Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero.

00004068 RUPC_P0 RX Unicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000406C RMPC_P0 RX Multicast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004070 RBPC_P0 RX Broadcast Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004074 RAEPC_P0 RX Alignment Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted.

00004078 RCEPC_P0 RX CRC(FCS) Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted.

0000407C RUSPC_P0 RX Undersize Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	The total number of packets received that are less than 64 octets long excluding framing bits, but including FCS octets which are otherwise well formed.

00004080 RFEPC_P0 RX Fragment Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).

00004084 ROSPC_P0 RX Oversize Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error.

00004088 RJEP_C_P0 RX Jabber Error Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).

0000408C RPPC_P0 RX Pause Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame.

00004090 RL64PC_P0 RX packet Length in 64-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.

00004094 RL65PC_P0 RX packet Length in 65-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004098 RL128PC_P0 RX packet Length in 128-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000409C RL256PC_P0 RX packet Length in 256-byte slot Packet Counter 00000000
of Port 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000040A0 RL512PC_P0 RX packet Length in 512-byte slot Packet Counter 00000000
of Port 0

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000040A4 RL1024PC_P0 RX packet Length in 1024-byte slot Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000040A8 ROCL_P0 RX Octet Counter Low double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000040AC ROCH_P0 Rx Octet Counter High double word of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above)

000040B0 RDPC_CTRL_P0 RX CTRL Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000040B4 RDPC_ING_P0 RX Ingress Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped according to the ingress rate limit set by the Ingress rate limiter

000040B8 RDPC_ARL_P0 RX ARL Drop Packet Counter of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000040D0				TX Port MIB Counter Half Full Status of Port 0										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status 0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status 0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000040D4 RMIB_HF_STS_P0 RX Port MIB Counter Half Full Status of Port 0 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True
18	RXOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	RXL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	RXL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	RXL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	RXL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	RXL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	RXL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	RXPAU_HF_STS	RX Pause Packet Counter Half Full Status 0: False 1: True
10	RXJAB_HF_STS	RX Jabber Error Counter Half Full Status 0: False 1: True
9	RXOVR_HF_STS	RX Oversize Packet Counter Half Full Status 0: False 1: True
8	RXFRG_HF_STS	RX Fragment Error Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
7	RXUND_HF_STS	RX Undersize Packet Counter Half Full Status 0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status 0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status 0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status 0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status 0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status 0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status 0: False 1: True
0	RXDROP_HF_STS	RX DROP Counter Half Full Status 0: False 1: True

00004100		TDPC P1		TX Drop Packet Counter of Port 1												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	TX_DROP_CNT																
Type	RO																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event when the frame output should be dropped due to the late collision or excessive collision

00004104 TCRC_P1 TX CRC Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004108 TUPC_P1 TX Unicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission

0000410C TMPC_P1 TX Multicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004110 TBPC_P1 TX Broadcast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

00004114 **TCEC P1** TX Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	The total number of collision events occurred during frame transmission

00004118 **TSEEC P1** TX Single Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	The number of frames transmitted without any error following a single collision

Bit(s)	Name	Description

0000411C **TMCEC_P1** TX Multiple Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	The number of frames transmitted without any error following multiple collisions

00004120 **TDEC_P1** TX Deferred Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode
		Frame involved in collision is not counted.

Bit(s)	Name	Description

00004124 **TLCEC P1** TX Late Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_LCOL_CNT The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004128 **TXCEC P1** TX excessive Collision Event Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_XCOL_CNT The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000412C TPPC_P1 TX Pause Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correctly transmitted MAC flow-control frame

00004130 TL64PC_P1 TX packet Length in 64-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004134 TL65PC_P1 TX packet Length in 65-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004138 TL128PC_P1 TX packet Length in 128-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000413C TL256PC_P1 TX packet Length in 256-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.

00004140 TL512PC_P1 TX packet Length in 512-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

00004144 TL1024PC_P1 TX packet Length in 1024-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

00004148 TOCL_P1 TX Octet Counter Low double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

Bit(s)	Name	Description

0000414C **TOCH_P1** TX Octet Counter High double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004160 **RDPC_P1** RX Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter

Bit(s)	Name	Description
3. broadcast Storm Control, trTCM or ACL Rate Limit		

00004164 **RFPC_P1** **RX Filtering Packet Counter of Port 1** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or when the port map is equal to zero

00004168 **RUPC_P1** **RX Unicast Packet Counter of Port 1** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000416C RMPC_P1 RX Multicast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004170 RBPC_P1 RX Broadcast Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004174 **RAEPC_P1** RX Alignment Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted

00004178 **RCEPC_P1** RX CRC(FCS) Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted

0000417C RUSPC_P1 RX Undersize Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDSIZE_CNT	The total number of packets received that are less than 64 octets long excluding framing bits, but including FCS octets which are otherwise well formed

00004180 RFEPC_P1 RX Fragment Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error).

00004184 ROSPC_P1 RX Oversize Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error

00004188 RJEPC_P1 RX Jabber Error Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

0000418C RPPC_P1 RX Pause Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame

00004190 RL64PC_P1 RX packet Length in 64-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received and equal to 64 octets in length, excluding framing bits but including FCS octets.

00004194 RL65PC_P1 RX packet Length in 65-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004198 RL128PC_P1 RX packet Length in 128-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received and transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000419C RL256PC_P1 RX packet Length in 256-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000041A0 RL512PC_P1 RX packet Length in 512-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000041A4 RL1024PC_P1 RX packet Length in 1024-byte slot Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000041A8 ROCL_P1 RX Octet Counter Low double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000041AC ROCH_P1 Rx Octet Counter High double word of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above)

000041B0 RDPC_CTRL_P1 RX CTRL Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000041B4 RDPC_ING_P1 RX Ingress Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter

000041B8 RDPC_ARL_P1 RX ARL Drop Packet Counter of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000041D0 **TMIB_HF_STS_P1** TX Port MIB Counter Half Full Status of Port 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status 0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status 0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000041D4		RMIB_HF_STS_P1				RX Port MIB Counter Half Full Status of Port 1										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS	
Type											W1C	W1C	W1C	W1C	W1C	W1C	
Reset											0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS	
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
18	R XOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	R XL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	R XL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	R XL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	R XL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	R XL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	R XL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	R XPAU_HF_STS	RX Pause Packet Counter Half Full Status 0: False 1: True
10	R XJAB_HF_STS	RX Jabber Error Counter Half Full Status 0: False 1: True
9	R XOVR_HF_STS	RX Oversize Packet Counter Half Full Status 0: False 1: True
8	R XFRG_HF_STS	RX Fragment Error Counter Half Full Status 0: False 1: True
7	R XUND_HF_STS	RX Undersize Packet Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status 0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status 0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status 0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status 0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status 0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status 0: False 1: True
0	RXDROP_HF_STS	RX DROP Counter Half Full Status 0: False 1: True

00004200	TDPC_P2				TX Drop Packet Counter of Port 2												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	TX_DROP_CNT																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	TX_DROP_CNT																	
Type	RO																	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event which the frame should be dropped on output due to the late collision or excessive collision

00004204	TCRC_P2		TX CRC Packet Counter of Port 2												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004208	TUPC_P2		TX Unicast Packet Counter of Port 2												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error, which excludes Pause frame but includes MAC control and successful retransmission

0000420C **TMPC_P2** TX Multicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004210 **TBPC_P2** TX Broadcast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

Bit(s)	Name	Description

00004214 TCEC_P2 TX Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_COL_CNT The total number of collision events occurrence during frame transmission

00004218 TSCEC_P2 TX Single Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_SCOL_CNT The number of frames transmitted without any error following a single collision

0000421C TMCEC_P2 TX Multiple Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	The number of frames transmitted without any error following multiple collisions

00004220 TDEC_P2 TX Deferred Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.

00004224 TLCEC_P2 TX Late Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004228 TXCEC_P2 TX excessive Collision Event Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000422C TPPEC_P2 TX Pause Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correctly transmitted MAC flow-control frame

00004230 TL64PC P2 TX packet Length in 64-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004234 TL65PC P2 TX packet Length in 65-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004238 TL128PC_P2 TX packet Length in 128-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000423C TL256PC_P2 TX packet Length in 256-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.

00004240 TL512PC_P2 TX packet Length in 512-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

00004244 TL1024PC_P2 TX packet Length in 1024-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

00004248 TOCL P2 TX Octet Counter Low double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000424C TOCH P2 TX Octet Counter High double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004260 RDPC_P2 RX Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit

00004264 RFPC_P2 RX Filtering Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero

00004268 RUPC_P2 RX Unicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000426C RMPC_P2 RX Multicast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004270 RBPC_P2 RX Broadcast Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004274 RAEPC_P2 RX Alignment Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted

00004278 RCEPC_P2 RX CRC(FCS) Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted

0000427C RUSPC_P2 RX Undersize Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed

00004280 RFEPC_P2 RX Fragment Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

00004284 ROSPC_P2 RX Oversize Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error

00004288 RJEP2 RX Jabber Error Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets, excluding framing bits but including FCS octets, and have either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

0000428C RPPC P2 RX Pause Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame

00004290 RL64PC_P2 RX packet Length in 64-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.

00004294 RL65PC_P2 RX packet Length in 65-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004298 RL128PC_P2 RX packet Length in 128-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000429C RL256PC_P2 RX packet Length in 256-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000042A0 RL512PC_P2 RX packet Length in 512-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000042A4 RL1024PC_P2 RX packet Length in 1024-byte slot Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000042A8 ROCL_P2 RX Octet Counter Low double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000042AC ROCH_P2 Rx Octet Counter High double word of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above).

000042B0 RDPC_CTRL_P2 RX CTRL Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000042B4 RDPC_ING_P2 RX Ingress Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter

000042B8 RDPC_ARL_P2 RX ARL Drop Packet Counter of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000042D0 TMIB_HF_STS_P2 TX Port MIB Counter Half Full Status of Port 2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDRO_P_HF_STS

Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status 0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status 0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000042D4	<u>RMIB_HF_STS_P2</u>				RX Port MIB Counter Half Full Status of Port 2						00000000					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True
18	RXOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	RXL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	RXL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	RXL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	RXL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	RXL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	RXL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
11	RXPAU_HF_STS	RX Pause Packet Counter Half Full Status
		0: False 1: True
10	RXJAB_HF_STS	RX Jabber Error Counter Half Full Status
		0: False 1: True
9	RXOVR_HF_STS	RX Oversize Packet Counter Half Full Status
		0: False 1: True
8	RXFRG_HF_STS	RX Fragment Error Counter Half Full Status
		0: False 1: True
7	RXUND_HF_STS	RX Undersize Packet Counter Half Full Status
		0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status
		0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status
		0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status
		0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status
		0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status
		0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status
		0: False 1: True

Bit(s)	Name	Description
0	RXDROP_HF_STS	RX DROP Counter Half Full Status
		0: False 1: True

00004300 **TDPC_P3** TX Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event which the frame should be dropped on output due to late collision or excessive collision

00004304 **TCRC_P3** TX CRC Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004308 **TUPC_P3** TX Unicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.

0000430C **TMPC_P3** TX Multicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004310 **TBPC_P3** **TX Broadcast Packet Counter of Port 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

00004314 **TCEC_P3** **TX Collision Event Counter of Port 3** **00000000**

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	The total number of collision events occurrence during frame transmission

Bit(s)	Name	Description

00004318 TSCEC_P3 TX Single Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_SCOL_CNT The number of frames transmitted without any error following a single collision

0000431C TMCEC_P3 TX Multiple Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_MCOL_CNT The number of frames transmitted without any error following multiple collisions

00004320 TDEC P3 TX Deferred Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.

00004324 TLCEC P3 TX Late Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004328 TXCEC P3 TX excessive Collision Event Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000432C TPPC_P3 TX Pause Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correct transmitted MAC flow-control frame

00004330 TL64PC_P3 TX packet Length in 64-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted and equal to 64 octets in length, and excluding framing bits but including FCS octets.

00004334 TL65PC_P3 TX packet Length in 65-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, and excluding framing bits but including FCS octets.

00004338 TL128PC_P3 TX packet Length in 128-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, and excluding framing bits but including FCS octets.

0000433C TL256PC_P3 TX packet Length in 256-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, and excluding framing bits but including FCS octets.

00004340 TL512PC_P3 TX packet Length in 512-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, and excluding framing bits but including FCS octets.

00004344 TL1024PC_P3 TX packet Length in 1024-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, and excluding framing bits but including FCS octets.

00004348 TOCL_P3 TX Octet Counter Low double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000434C TOCH_P3 TX Octet Counter High double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004360 RDPC_P3 RX Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004364 RFPC_P3 RX Filtering Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero

00004368 RUPC_P3 RX Unicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000436C RMPC P3 RX Multicast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004370 RBPC P3 RX Broadcast Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004374 RAEPC_P3 RX Alignment Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted

00004378 RCEPC_P3 RX CRC(FCS) Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted

0000437C RUSPC_P3 RX Undersize Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed

00004380 RFEPC_P3 RX Fragment Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

00004384 ROSPC_P3 RX Oversize Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error

00004388 RJEP3 RX Jabber Error Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

0000438C RPPC_P3 RX Pause Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame

00004390 RL64PC_P3 RX packet Length in 64-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.

00004394 RL65PC_P3 RX packet Length in 65-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004398 RL128PC_P3 RX packet Length in 128-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000439C RL256PC P3 RX packet Length in 256-byte slot Packet Counter 00000000
of Port 3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000043A0 RL512PC P3 RX packet Length in 512-byte slot Packet Counter 00000000
of Port 3

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000043A4 RL1024PC_P3 RX packet Length in 1024-byte slot Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000043A8 ROCL_P3 RX Octet Counter Low double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000043AC ROCH_P3 Rx Octet Counter High double word of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above).

000043B0 RDPC_CTRL_P3 RX CTRL Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000043B4 RDPC_ING_P3 RX Ingress Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter

000043B8 RDPC_ARL_P3 RX ARL Drop Packet Counter of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000043D0 TMIB_HF_STS_P3 TX Port MIB Counter Half Full Status of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status 0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status 0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000043D4 RMIB_HF_STS_P3 RX Port MIB Counter Half Full Status of Port 3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL102_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True
18	RXOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	RXL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	RXL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	RXL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	RXL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	RXL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	RXL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	RXPAU_HF_STS	RX Pause Packet Counter Half Full Status 0: False 1: True
10	RXJAB_HF_STS	RX Jabber Error Counter Half Full Status 0: False 1: True
9	RXOVR_HF_STS	RX Oversize Packet Counter Half Full Status 0: False 1: True
8	RXFRG_HF_STS	RX Fragment Error Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
7	RXUND_HF_STS	RX Undersize Packet Counter Half Full Status 0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status 0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status 0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status 0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status 0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status 0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status 0: False 1: True
0	RXDROP_HF_STS	RX DROP Counter Half Full Status 0: False 1: True

00004400		TDPC P4				TX Drop Packet Counter of Port 4											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	TX_DROP_CNT																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event which the frame should be dropped on output due to the late collision or excessive collision.

00004404 TCRC_P4 TX CRC Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004408 TUPC_P4 TX Unicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.

0000440C TMPC_P4 TX Multicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004410 TBPC_P4 TX Broadcast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

00004414 **TCEC P4** TX Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	The total number of collision events occurrence during frame transmission

00004418 **TSCEC P4** TX Single Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_SCOL_CNT	The number of frames transmitted without any error following a single collision

Bit(s)	Name	Description

0000441C **TMCEC_P4** TX Multiple Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	The number of frames transmitted without any error following multiple collisions

00004420 **TDEC_P4** TX Deferred Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.

Bit(s)	Name	Description

00004424 **TLCEC P4** TX Late Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004428 **TXCEC P4** TX excessive Collision Event Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000442C TPPC_P4 TX Pause Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correct transmitted MAC flow-control frame

00004430 TL64PC_P4 TX packet Length in 64-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004434 TL65PC_P4 TX packet Length in 65-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004438 TL128PC_P4 TX packet Length in 128-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000443C TL256PC_P4 TX packet Length in 256-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.

00004440 TL512PC_P4 TX packet Length in 512-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

00004444 TL1024PC_P4 TX packet Length in 1024-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

00004448 TOCL_P4 TX Octet Counter Low double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

Bit(s)	Name	Description

0000444C **TOCH P4** TX Octet Counter High double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004460 **RDPC P4** RX Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter

Bit(s)	Name	Description
3. broadcast Storm Control, trTCM or ACL Rate Limit .		

00004464 RFPC_P4 RX Filtering Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero

00004468 RUPC_P4 RX Unicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000446C RMPC_P4 RX Multicast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004470 RBPC_P4 RX Broadcast Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004474 RAEPC_P4 RX Alignment Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted

00004478 RCEPC_P4 RX CRC(FCS) Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted

0000447C **RUSPC_P4** RX Undersize Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDSIZE_CNT	The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed.

00004480 **RFEPC_P4** RX Fragment Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

00004484 ROSPC_P4 RX Oversize Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error

00004488 RJEP_C_P4 RX Jabber Error Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

0000448C RPPC_P4 RX Pause Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame

00004490 RL64PC_P4 RX packet Length in 64-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.

00004494 RL65PC_P4 RX packet Length in 65-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004498 RL128PC_P4 RX packet Length in 128-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000449C RL256PC_P4 RX packet Length in 256-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000044A0 RL512PC_P4 RX packet Length in 512-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000044A4 RL1024PC_P4 RX packet Length in 1024-byte slot Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000044A8 ROCL_P4 RX Octet Counter Low double word of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000044AC	ROCH_P4				Rx Octet Counter High double word of Port 4												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	RX_OCT_CNT_H																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	RX_OCT_CNT_H																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above).

000044B0	RDPC_CTRL_P4				RX CTRL Drop Packet Counter of Port 4												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	RX_CTRL_DROP_CNT																	
Type	RO																	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	RX_CTRL_DROP_CNT																	
Type	RO																	

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000044B4 RDPC_ING_P4 RX Ingress Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter

000044B8 RDPC_ARL_P4 RX ARL Drop Packet Counter of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000044D0 **TMIB_HF_STS_P4** TX Port MIB Counter Half Full Status of Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status 0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status 0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000044D4				RMIB HF_STS_P4				RX Port MIB Counter Half Full Status of Port 4								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS			
Type											W1C	W1C	W1C	W1C	W1C	W1C			
Reset											0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDROP_HF_STS			
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
18	R XOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	R XL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	R XL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	R XL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	R XL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	R XL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	R XL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	R XPAU_HF_STS	RX Pause Packet Counter Half Full Status 0: False 1: True
10	R XJAB_HF_STS	RX Jabber Error Counter Half Full Status 0: False 1: True
9	R XOVR_HF_STS	RX Oversize Packet Counter Half Full Status 0: False 1: True
8	R XFRG_HF_STS	RX Fragment Error Counter Half Full Status 0: False 1: True
7	R XUND_HF_STS	RX Undersize Packet Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status
		0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status
		0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status
		0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status
		0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status
		0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status
		0: False 1: True
0	RXDROP_HF_STS	RX DROP Counter Half Full Status
		0: False 1: True

00004500		TDPC_P5				TX Drop Packet Counter of Port 5										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	TX_DROP_CNT																
Type	RO																
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name	TX_DROP_CNT																
Type	RO																

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event which the frame should be dropped on output due to the late collision or excessive collision

00004504 TCRC_P5 TX CRC Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004508 TUPC_P5 TX Unicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.

0000450C **TMPC_P5** TX Multicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004510 **TBPC_P5** TX Broadcast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

Bit(s)	Name	Description

00004514 **TCEC_P5** TX Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_COL_CNT The total number of collision events occurrence during frame transmission

00004518 **TSCEC_P5** TX Single Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_SCOL_CNT The number of frames transmitted without any error following a single collision

0000451C TMCEC_P5 TX Multiple Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCOL_CNT	The number of frames transmitted without any error following multiple collisions

00004520 TDEC_P5 TX Deferred Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.

00004524 TLCEC_P5 TX Late Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004528 TXCEC_P5 TX excessive Collision Event Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000452C TPPEC_P5 TX Pause Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correct transmitted MAC flow-control frame

00004530 TL64PC_P5 TX packet Length in 64-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004534 TL65PC_P5 TX packet Length in 65-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004538 TL128PC_P5 TX packet Length in 128-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000453C TL256PC_P5 TX packet Length in 256-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.

00004540 TL512PC_P5 TX packet Length in 512-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

00004544 TL1024PC_P5 TX packet Length in 1024-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

00004548 TOCL P5 TX Octet Counter Low double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000454C TOCH P5 TX Octet Counter High double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004560 RDPC_P5 RX Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004564 RFPC_P5 RX Filtering Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero

00004568 RUPC_P5 RX Unicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000456C RMPC_P5 RX Multicast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004570 RBPC_P5 RX Broadcast Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004574 RAEPC_P5 RX Alignment Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted

00004578 RCEPC_P5 RX CRC(FCS) Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted

0000457C RUSPC_P5 RX Undersize Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed

00004580 RFEPC_P5 RX Fragment Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

00004584 ROSPC_P5 RX Oversize Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error

00004588 RJEP_C P5 RX Jabber Error Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

0000458C RPPC P5 RX Pause Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame

00004590 RL64PC_P5 RX packet Length in 64-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.

00004594 RL65PC_P5 RX packet Length in 65-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004598 RL128PC_P5 RX packet Length in 128-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000459C RL256PC_P5 RX packet Length in 256-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000045A0 RL512PC_P5 RX packet Length in 512-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000045A4 RL1024PC_P5 RX packet Length in 1024-byte slot Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000045A8 ROCL_P5 RX Octet Counter Low double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000045AC ROCH_P5 Rx Octet Counter High double word of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above).

000045B0 RDPC_CTRL_P5 RX CTRL Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000045B4 RDPC_ING_P5 RX Ingress Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter

000045B8 RDPC_ARL_P5 RX ARL Drop Packet Counter of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000045D0 TMIB_HF_STS_P5 TX Port MIB Counter Half Full Status of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDRO_P_HF_STS

Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status 0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status 0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000045D4 RMIB_HF_STS_P5 RX Port MIB Counter Half Full Status of Port 5 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL102_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True
18	RXOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	RXL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	RXL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	RXL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	RXL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	RXL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	RXL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
11	RXPAU_HF_STS	RX Pause Packet Counter Half Full Status
		0: False 1: True
10	RXJAB_HF_STS	RX Jabber Error Counter Half Full Status
		0: False 1: True
9	RXOVR_HF_STS	RX Oversize Packet Counter Half Full Status
		0: False 1: True
8	RXFRG_HF_STS	RX Fragment Error Counter Half Full Status
		0: False 1: True
7	RXUND_HF_STS	RX Undersize Packet Counter Half Full Status
		0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status
		0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status
		0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status
		0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status
		0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status
		0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status
		0: False 1: True

Bit(s)	Name	Description
0	RXDROP_HF_STS	RX DROP Counter Half Full Status
		0: False 1: True

00004600 **TDPC_P6** TX Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DROP_CNT	The number of event which the frame should be dropped on output due to the late collision or excessive collision

00004604 **TCRC_P6** TX CRC Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_CRC_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_CRC_CNT	The number of event which the frame will output a CRC packet due to TX FIFO underrun

00004608 **TUPC_P6** TX Unicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_UCAST_CNT	The number of unicast frames transmitted without any error. It excludes Pause frame but includes MAC control and successful retransmission.

0000460C **TMPC_P6** TX Multicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_MCAST_CNT	The number of multicast frames transmitted without any error

00004610 **TBPC_P6** TX Broadcast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_BCAST_CNT	The number of broadcast frames transmitted without any error

00004614 **TCEC_P6** TX Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_COL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_COL_CNT	The total number of collision events occurrence during frame transmission

Bit(s)	Name	Description

00004618 **TSCEC P6** TX Single Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_SCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_SCOL_CNT The number of frames transmitted without any error following a single collision

0000461C **TMCEC P6** TX Multiple Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_MCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description

31:0 TX_MCOL_CNT The number of frames transmitted without any error following multiple collisions

00004620 TDEC P6 TX Deferred Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_DEFER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_DEFER_CNT	The number of frames deferred at the first transmit attempt due to a busy medium in half duplex mode. Frame involved in collision is not counted.

00004624 TLCEC P6 TX Late Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_LCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_LCOL_CNT	The number of transmission abortion due to a collision occurring after the transmission of the first 64 bytes for that packet

00004628 TXCEC P6 TX excessive Collision Event Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_XCOL_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_XCOL_CNT	The number of frames that have experienced MAX_COL_NUM (default 16) consecutive collisions or more, not including late collisions

0000462C TPPC_P6 TX Pause Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PAUSE_CNT	The number of correct transmitted MAC flow-control frame

00004630 TL64PC_P6 TX packet Length in 64-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_64_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_64_CNT	It indicates the total number of packets, including bad packets transmitted equal to 64 octets in length, excluding framing bits but including FCS octets.

00004634 TL65PC_P6 TX packet Length in 65-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets transmitted between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004638 TL128PC_P6 TX packet Length in 128-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_128TO255_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000463C TL256PC_P6 TX packet Length in 256-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets transmitted between 256 and 511 octets in length, excluding framing bits but including FCS octets.

00004640 TL512PC_P6 TX packet Length in 512-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_512TO1023_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets transmitted between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

00004644 TL1024PC_P6 TX packet Length in 1024-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets transmitted between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

00004648 TOCL_P6 TX Octet Counter Low double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_L															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_L	{TX_OCT_CNT_H, TX_OCT_CNT_L} represents the number of bytes transmitted in good or bad frames, excluding preamble bits but including FCS octets. TX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. TX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. TX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. TX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

0000464C TOCH P6 TX Octet Counter High double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	TX_OCT_CNT_H	Refer to TX_OCT_CNT_L (above).

00004660 RDPC P6 RX Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_DROP_CNT	The number of event which the frame should be dropped due to 1. an internal buffer shortage by RX_CTRL 2. ingress rate limit by Ingress rate limiter 3. broadcast Storm Control, trTCM or ACL Rate Limit .

00004664 RFPC_P6 RX Filtering Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FILTER_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FILTER_CNT	The number of frames which is filtered by ARL module due to ARL security, length error, control frame, or port map is equal to zero

00004668 RUPC_P6 RX Unicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UCAST_CNT	The number of unicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

0000466C RMPC P6 RX Multicast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_MCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_MCAST_CNT	The number of multicast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004670 RBPC P6 RX Broadcast Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_BCAST_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_BCAST_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_BCAST_CNT	The number of broadcast frames with length between 64 bytes and the maximum frame size, received without any error, including MAC control frames

00004674 RAEPC_P6 RX Alignment Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ALIGN_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ALIGN_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with a non-integral number of bytes and a CRC error or RX_ER asserted

00004678 RCEPC_P6 RX CRC(FCS) Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FCS_ERR_CNT															
Type	RO															

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FCS_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FCS_ERR_CNT	The number of frames with length between 64 bytes and the maximum frame size, received with an integral number of bytes and a CRC error or RX_ER asserted

0000467C RUSPC_P6 RX Undersize Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_UNDERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_UNDERSIZE_CNT	The total number of packets received that are less than 64 octets long, excluding framing bits but including FCS octets which are otherwise well formed

00004680 RFEPC_P6 RX Fragment Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_FRAG_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_FRAG_ERR_CNT	The total number of packets received that are less than 64 octets in length, excluding framing bits but including FCS octets and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

00004684 ROSPC_P6 RX Oversize Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OVERSIZE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OVERSIZE_CNT	The number of frames with length larger than the maximum frame size, received without any error

00004688 RJEP_C P6 RX Jabber Error Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_JABB_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_JABB_ERR_CNT	The total number of packets received that are longer than 1518 octets excluding framing bits, but including FCS octets, and had either a bad Frame Check Sequence (FCS) with an integral number of octets (FCS Error) or a bad FCS with a non-integral number of octets (Alignment Error)

0000468C RPPC_P6 RX Pause Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PAUSE_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PAUSE_CNT	The number of correctly received MAC flow-control frame

00004690 RL64PC_P6 RX packet Length in 64-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_64_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_64_CNT	It indicates the total number of packets, including bad packets received equal to 64 octets in length, excluding framing bits but including FCS octets.

00004694 RL65PC_P6 RX packet Length in 65-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_65TO127_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_65TO127_CNT	It indicates the total number of packets, including bad packets received between 65 and 127 octets in length, excluding framing bits but including FCS octets.

00004698 RL128PC_P6 RX packet Length in 128-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_128TO255_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_128TO255_CNT	It indicates the total number of packets, including bad packets received transmitted between 128 and 255 octets in length, excluding framing bits but including FCS octets.

0000469C RL256PC_P6 RX packet Length in 256-byte slot Packet Counter 00000000
of Port 6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_256TO511_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_256TO511_CNT	It indicates the total number of packets, including bad packets received between 256 and 511 octets in length, excluding framing bits but including FCS octets.

000046A0 RL512PC_P6 RX packet Length in 512-byte slot Packet Counter 00000000
of Port 6

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_PKT_512TO1023_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_512TO1023_CNT	It indicates the total number of packets, including bad packets received between 512 and 1023 octets in length, excluding framing bits but including FCS octets.

000046A4 RL1024PC_P6 RX packet Length in 1024-byte slot Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_PKT_1024TOMAX_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_PKT_1024TOMAX_CNT	It indicates the total number of packets, including bad packets received between 1024 and MAX_FRAME_SIZE octets in length, excluding framing bits but including FCS octets.

000046A8 ROCL_P6 RX Octet Counter Low double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	RX_OCT_CNT_L															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_L	{RX_OCT_CNT_H, RX_OCT_CNT_L} represents the number of bytes received in good or bad frames, excluding preamble bits but including FCS octets. RX_OCT_CNT_GOOD bit = 1 (enabled), good packet bytes counted. RX_OCT_CNT_GOOD bit = 0 (disabled), good packet bytes not counted. RX_OCT_CNT_BAD bit = 1 (enabled), bad packet bytes counted. RX_OCT_CNT_BAD bit = 0 (disabled), bad packet bytes not counted.

000046AC ROCH_P6 Rx Octet Counter High double word of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_OCT_CNT_H															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_OCT_CNT_H	Refer to RX_OCT_CNT_L (above).

000046B0 RDPC_CTRL_P6 RX CTRL Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_CTRL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_CTRL_DROP_CNT	The number of event which the frame should be dropped due to error interrupt issued by RX_CTRL

000046B4 RDPC_ING_P6 RX Ingress Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ING_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ING_DROP_CNT	The number of event which the frame should be dropped due to a ingress rate limit by Ingress rate limiter

000046B8 RDPC_ARL_P6 RX ARL Drop Packet Counter of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	RX_ARL_DROP_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RX_ARL_DROP_CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	RX_ARL_DROP_CNT	The number of event which the frame should be dropped due to broadcast Storm Control, trTCM or ACL Rate Limit

000046D0				TX Port MIB Counter Half Full Status of Port 6										00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name														TXOCT_HF_STS	TXL1024_HF_STS	TXL512_HF_STS
Type														W1C	W1C	W1C
Reset														0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TXL256_HF_STS	TXL128_HF_STS	TXL65_HF_STS	TXL64_HF_STS	TXPAU_HF_STS	TXECOL_HF_STS	TXLCOL_HF_STS	TXDFR_HF_STS	TXMCO_L_HF_STS	TXSCOL_HF_STS	TXCOL_HF_STS	TXBRD_HF_STS	TXMUL_HF_STS	TXUNI_HF_STS	TXCRC_HF_STS	TXDROP_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
18	TXOCT_HF_STS	TX Octet Counter Half Full Status 0: False 1: True
17	TXL1024_HF_STS	TX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	TXL512_HF_STS	TX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	TXL256_HF_STS	TX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
14	TXL128_HF_STS	TX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	TXL65_HF_STS	TX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	TXL64_HF_STS	TX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	TXPAU_HF_STS	TX Pause Packet Counter Half Full Status 0: False 1: True
10	TXECOL_HF_STS	TX Excessive Collision Counter Half Full Status 0: False 1: True
9	TXLCOL_HF_STS	TX Late Collision Counter Half Full Status 0: False 1: True
8	TXDFR_HF_STS	TX Deferred Counter Half Full Status 0: False 1: True
7	TXMCOL_HF_STS	TX Multiple Collision Counter Half Full Status 0: False 1: True
6	TXSCOL_HF_STS	TX Single Collision Counter Half Full Status 0: False 1: True
5	TXCOL_HF_STS	TX Collision Event Counter Half Full Status 0: False 1: True
4	TXBRD_HF_STS	TX Broadcast Counter Half Full Status 0: False 1: True
3	TXMUL_HF_STS	TX Multicast Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
2	TXUNI_HF_STS	TX Unicast Counter Half Full Status 0: False 1: True
1	TXCRC_HF_STS	TX CRC Counter Half Full Status 0: False 1: True
0	TXDROP_HF_STS	TX DROP Counter Half Full Status 0: False 1: True

000046D4 RMIB_HF_STS_P6 RX Port MIB Counter Half Full Status of Port 6 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RXARL_HF_STS	RXING_HF_STS	RXCTRL_HF_STS	RXOCT_HF_STS	RXL1024_HF_STS	RXL512_HF_STS
Type											W1C	W1C	W1C	W1C	W1C	W1C
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RXL256_HF_STS	RXL128_HF_STS	RXL65_HF_STS	RXL64_HF_STS	RXPAU_HF_STS	RXJAB_HF_STS	RXOVR_HF_STS	RXFRG_HF_STS	RXUND_HF_STS	RXCRC_HF_STS	RXALG_HF_STS	RXBRD_HF_STS	RXMUL_HF_STS	RXUNI_HF_STS	RXFIL_HF_STS	RXDRO_P_HF_STS
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21	RXARL_HF_STS	RX ARL Drop Counter Half Full Status 0: False 1: True
20	RXING_HF_STS	RX Ingress Drop Counter Half Full Status 0: False 1: True

Bit(s)	Name	Description
19	RXCTRL_HF_STS	RX CTRL Drop Counter Half Full Status 0: False 1: True
18	RXOCT_HF_STS	RX Octet Counter Half Full Status 0: False 1: True
17	RXL1024_HF_STS	RX Packet Length above 1024 Bytes Counter Half Full Status 0: False 1: True
16	RXL512_HF_STS	RX Packet Length 512 ~ 1023 Bytes Counter Half Full Status 0: False 1: True
15	RXL256_HF_STS	RX Packet Length 256 ~ 511 Bytes Counter Half Full Status 0: False 1: True
14	RXL128_HF_STS	RX Packet Length 128 ~ 255 Bytes Counter Half Full Status 0: False 1: True
13	RXL65_HF_STS	RX Packet Length 65 ~ 127 Bytes Counter Half Full Status 0: False 1: True
12	RXL64_HF_STS	RX Packet Length 64 Bytes Counter Half Full Status 0: False 1: True
11	RXPAU_HF_STS	RX Pause Packet Counter Half Full Status 0: False 1: True
10	RXJAB_HF_STS	RX Jabber Error Counter Half Full Status 0: False 1: True
9	RXOVR_HF_STS	RX Oversize Packet Counter Half Full Status 0: False 1: True
8	RXFRG_HF_STS	RX Fragment Error Counter Half Full Status

Bit(s)	Name	Description
		0: False 1: True
7	RXUND_HF_STS	RX Undersize Packet Counter Half Full Status 0: False 1: True
6	RXCRC_HF_STS	RX CRC ERROR Counter Half Full Status 0: False 1: True
5	RXALG_HF_STS	RX Alignment Error Counter Half Full Status 0: False 1: True
4	RXBRD_HF_STS	RX Broadcast Counter Half Full Status 0: False 1: True
3	RXMUL_HF_STS	RX Multicast Counter Half Full Status 0: False 1: True
2	RXUNI_HF_STS	RX Unicast Counter Half Full Status 0: False 1: True
1	RXFIL_HF_STS	RX Filtering Counter Half Full Status 0: False 1: True
0	RXDROP_HF_STS	RX DROP Counter Half Full Status 0: False 1: True

00004F00		<u>AE0CNT</u>				ACL Event 0 Counter										00000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE0CNT																
Type	RO																
Reset		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	AE0CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE0CNT	Total number of ARL event 0 occurred

00004F04 AE1CNT ACL Event 1 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE1CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE1CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE1CNT	Total number of ARL event 1 occurred

00004F08 AE2CNT ACL Event 2 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE2CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE2CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE2CNT	Total number of ARL event 2 occurred

00004F0C AE3CNT ACL Event 3 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE3CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE3CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE3CNT	Total number of ARL event 3 occurred

00004F10 AE4CNT ACL Event 4 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE4CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE4CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE4CNT	Total number of ARL event 4 occurred

00004F14 AE5CNT ACL Event 5 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE5CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE5CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE5CNT	Total number of ARL event 5 occurred

00004F18 AE6CNT ACL Event 6 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE6CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE6CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE6CNT	Total number of ARL event 6 occurred

00004F1C AE7CNT ACL Event 7 Counter 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AE7CNT															

Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	AE7CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	AE7CNT	Total number of ARL event 7 occurred

00004FE0				MIBCCR								MIB Counter Control				800000F0			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	MIB_ENABLE																		
Type	RW																		
Reset	1																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name									RX_OCT_CNT_GOOD	RX_OCT_CNT_BAD	TX_OCT_CNT_GOOD	TX_OCT_CNT_BAD							
Type									RW	RW	RW	RW							
Reset									1	1	1	1							

Bit(s)	Name	Description
31	MIB_ENABLE	1'b0: Disable MIB counter and set all counter values to zero. 1'b1: Enable MIB counter.
7	RX_OCT_CNT_GOOD	1'b0: Octets of good received packets are not counted in RX_OCT_L_CNT and RX_OCT_H_CNT. 1'b1: Octets of good received packets are counted in RX_OCT_L_CNT and RX_OCT_H_CNT.
6	RX_OCT_CNT_BAD	1'b0: Octets of bad received packets are not counted in RX_OCT_L_CNT and RX_OCT_H_CNT.

Bit(s)	Name	Description
		1'b1: Octets of bad received packets are counted in RX_OCT_L_CNT and RX_OCT_H_CNT.
5	TX_OCT_CNT_GOOD	1'b0: Octets of good transmitted packets are not counted in TX_OCT_L_CNT and TX_OCT_H_CNT. 1'b1: Octets of good transmitted packets are counted in TX_OCT_L_CNT and TX_OCT_H_CNT. Good transmitted packets are frames transmitted successfully.
4	TX_OCT_CNT_BAD	1'b0: Octets of bad transmitted packets are not counted in TX_OCT_L_CNT and TX_OCT_H_CNT. 1'b1: Octets of bad transmitted packets are counted in TX_OCT_L_CNT and TX_OCT_H_CNT. Bad transmitted packets are frames transmitted in collision with deliberately destroyed CRC.

00004FE4		AECR														80000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	AEC_ENABLE																
Type	RW																
Reset	1																
Bit		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																	
Type																	
Reset																	

Bit(s)	Name	Description
31	AEC_ENABLE	1'b0: Disable ARL event counter function and set all counter value to zero. 1'b1: Enable ARL event counter.

00004FE8		AEMIB HF_STS														00000000	
Bit		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																	

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name									ARLEV7_HF_STS	ARLEV6_HF_STS	ARLEV5_HF_STS	ARLEV4_HF_STS	ARLEV3_HF_STS	ARLEV2_HF_STS	ARLEV1_HF_STS	ARLEV0_HF_STS
Type									W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset									0	0	0	0	0	0	0	0

Bit(s)	Name	Description
7	ARLEV7_HF_STS	ARL Event 7 MIB Counter Half Full Status 0: False 1: True
6	ARLEV6_HF_STS	ARL Event 6 MIB Counter Half Full Status 0: False 1: True
5	ARLEV5_HF_STS	ARL Event 5 MIB Counter Half Full Status 0: False 1: True
4	ARLEV4_HF_STS	ARL Event 4 MIB Counter Half Full Status 0: False 1: True
3	ARLEV3_HF_STS	ARL Event 3 MIB Counter Half Full Status 0: False 1: True
2	ARLEV2_HF_STS	ARL Event 2 MIB Counter Half Full Status 0: False 1: True
1	ARLEV1_HF_STS	ARL Event 1 MIB Counter Half Full Status 0: False 1: True
0	ARLEV0_HF_STS	ARL Event 0 MIB Counter Half Full Status 0: False 1: True

00004FF0 MIBHF_INT_EN Port/ARL MIB Counter Half Full Interrupt Enable 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	HFSTS_ ARL_ E_ N															
Type	RW															
Reset	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										HFSTS_ P6_ EN	HFSTS_ P5_ EN	HFSTS_ P4_ EN	HFSTS_ P3_ EN	HFSTS_ P2_ EN	HFSTS_ P1_ EN	HFSTS_ P0_ EN
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31	HFSTS_ ARL_ EN	ARL MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable
6	HFSTS_ P6_ EN	Port 6 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable
5	HFSTS_ P5_ EN	Port 5 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable
4	HFSTS_ P4_ EN	Port 4 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable

Bit(s)	Name	Description
3	HFSTS_P3_EN	Port 3 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable
2	HFSTS_P2_EN	Port 2 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable
1	HFSTS_P1_EN	Port 1 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable
0	HFSTS_P0_EN	Port 0 MIB Half Full Interrupt Enable. When this function is enabled, and the half full status is on, the switch will enable an interrupt signal for software. 0: Disable 1: Enable

00004FF4		MIBHF_INT_STS				Port/ARL MIB Counter Half Full Interrupt Status											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name	HFSTS_ARL																	
Type	W1C																	
Reset	0																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name										HFSTS_P6	HFSTS_P5	HFSTS_P4	HFSTS_P3	HFSTS_P2	HFSTS_P1	HFSTS_P0		
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C		
Reset										0	0	0	0	0	0	0		

Bit(s)	Name	Description
31	HFSTS_ARL	ARL MIB Half Full Interrupt Status 0: False 1: True
6	HFSTS_P6	Port 6 MIB Half Full Interrupt Status 0: False 1: True
5	HFSTS_P5	Port 5 MIB Half Full Interrupt Status 0: False 1: True
4	HFSTS_P4	Port 4 MIB Half Full Interrupt Status 0: False 1: True
3	HFSTS_P3	Port 3 MIB Half Full Interrupt Status 0: False 1: True
2	HFSTS_P2	Port 2 MIB Half Full Interrupt Status 0: False 1: True
1	HFSTS_P1	Port 1 MIB Half Full Interrupt Status 0: False 1: True
0	HFSTS_P0	Port 0 MIB Half Full Interrupt Status 0: False 1: True

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7 Serial Gigabit Media Independent Interface (SGMII)

7.1 Introduction

The SGMII is the interface between 10/100/1000/2500 Mbps PHY and Ethernet MAC, the spec is raised by Cisco in 1999, which is aims for pin reduction compare with the GMII. It uses 2 differential data pair for TX and RX with clock embedded bit stream to convey frame data and port ability information. The core leverages the 1000Base-X PCS and Auto-Negotiation from IEEE 802.3 specification (clause 36/37). This IP can support up to 3.125G baud for 2.5Gbps (proprietary 2500Base-X) data rate of MAC by overclocking.

7.2 Features

- Support 10/100/1000/2500 Mbps in full duplex mode and 10/100 Mbps in half duplex mode
- Support programmable Link timer
- Support I2C interface for accessing
- Support internal pattern generator with PRBS-7/ clock / user defined pattern for testing
- Support PCS/SERDES level loopback path in transmit/receive direction for system debugging
- Support auto initialization for dumb-switch (auto force to 2500Mbps mode)

7.3 Block Diagram

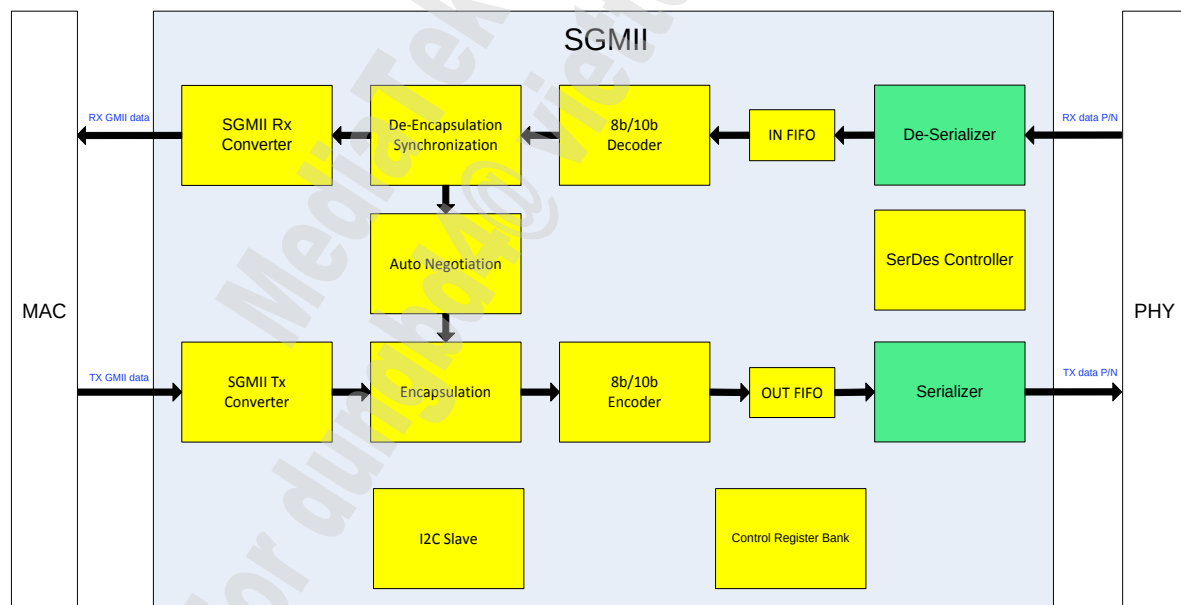


Figure 7-1. Block diagram of SGMII

7.4 SGMII AN/force mode setting guide

In MT7531, users can follow settings below to program SGMII into Auto-Negotiation (AN) mode or force mode. In Auto-Negotiation mode, SGMII supports Auto-Negotiation from IEEE 802.3 specification (clause 36/37). In force mode, user can force SGMII running at fixed speed & duplex mode.

7.4.1 Auto-Negotiation mode

1. Set PHYA into power down state
 - 0x50E8[4], set 1
2. Set Gen1 speed
 - 0x5128[2], set 0 : 1Gbps
3. Remote fault disable
 - 0x5020[8], set 1
4. Setting Link partner's AN enable = 1
5. Setting Link partner's device ability for speed/duplex
6. AN re-start
 - 0x5000[9], set 1
7. Release PHYA power down state
 - 0x50E8[4], set 0

7.4.2 Force mode

1. Set PHYA into power down state
 - 0x50E8[4], set 1
2. Decide Gen1 / Gen2 speed
 - 0x5128[2], set 0 : 1Gbps/100Mbps/10Mbps, 1 : 2.5Gbps
3. Disable AN
 - 0x5000[12], set 0
4. SGMII force mode setting
 - 0x5020[1], set 0
 - 0x5020[3:2], set 00 : 10Mbps, 01 : 100Mbps, 10 : 1000/2500Mbps, 11 : reserved
 - 0x5020[4], set 0 : full duplex, 1 : half duplex (if [3:2] = 10, it will force full duplex)
5. Disable Link partner's AN
6. Link partner's force mode setting
7. Release PHYA power down state
 - 0x50E8[4], set 0

7.5 Register Definition

Module name: sgmi_reg_0 Base address: (+0x00005000)

Address	Name	Width	Register Function
00005000	<u>PCS_CONTROL_1</u>	32	C45 3.1
00005004	<u>PCS_DEVICE_IDENTIFIER</u>	32	C45 3.3
00005008	<u>PCS_SPEED_ABILITY</u>	32	C45 3.5
0000500C	<u>PACKAGE_PRESENT</u>	32	C45 3.7
00005010	<u>PCS_STATUS_2</u>	32	C45 3.8
00005014	<u>PCS_SCRATCH</u>	32	
00005018	<u>PCS_LINK_TIMER</u>	32	
0000501C	<u>PCS_DEC_ERROR_CNT</u>	32	
00005020	<u>SGMII_MODE</u>	32	
00005024	<u>SGMII_RESERVED</u>	32	
0000502C	<u>SGMII_WO_REG_VALUE</u>	32	
00005034	<u>SGMII_RESERVED_0</u>	32	C45 3.2001
00005040	<u>SGMII_RW_0</u>	32	
0000504C	<u>INTERRUPT_CONTROL_0</u>	32	
00005050	<u>INTERRUPT_CONTROL_1</u>	32	
00005060	<u>QPHY_SIG_DET_CTRL</u>	32	QPHY signal detect threshold control
000050C4	<u>PAT_GEN_CTRL_0</u>	32	Pattern Gen control_0
000050C8	<u>PAT_GEN_CTRL_1</u>	32	Pattern Gen control_1
000050CC	<u>PAT_GEN_CTRL_2</u>	32	Pattern Gen control_2
000050D0	<u>PAT_GEN_CTRL_3</u>	32	Pattern Gen control_3
000050E8	<u>QPHY_PWR_STATE_CTRL</u>	32	QPHY power state control
000050EC	<u>QPHY_WRAP_CTRL</u>	32	QPHY wrapper control
000050F0	<u>I2C_CTRL</u>	32	I2C interface control

00005000		PCS_CONTROL_1				C45 3.1				00001140						
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SGMII_ AN_EX PANSI ON_CL R							SGMII_ PCS_FA ULT		SGMII_ AN_CO MPLET E		SGMII_ AN_ABI LITY	SGMII_ LINK_S TATUS		
Type		WO							RO		RO		RO	RO		
Reset		0							0		0		0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name				SGMII_ AN_EN ABLE		SGMII_ ISOLAT E	SGMII_ AN_RE START									
Type				RW		RW	WO									
Reset				1		0	0									

Bit(s)	Name	Description
30	SGMII_AN_EXPANSION_CLR	Page_Receive flag clear 1'b0 : no effect
23	SGMII_PCS_FAULT	1'b1 : reset @SGMII_AN_EXPANSION_12_0[1] to 0 SGMII fault condition detection 1'b0 : No fault condition detected
21	SGMII_AN_COMPLETE	1'b1 : Fault condition detected (txfifo_full or rxfifo_empty) AN complete 1'b0 : AN not complete
19	SGMII_AN_ABILITY	1'b1 : when @SGMII_AN_ENABLE=1, @SGMII_SW_RESET=0 and an_done is synchronized from rx_mii_ck to csr_ck Auto-Negotiation ability 1'b0 : PHY is not able to perform Auto-Negotiation
18	SGMII_LINK_STATUS	1'b1 : PHY is able to perform Auto-Negotiation Signal link_status 1'b0 : when loss of sync
12	SGMII_AN_ENABLE	1'b1 : when acquire sync (if SGMII_AN_ENABLE = 1, it will check if SGMII_AN_COMPLETE = 1 as well) Auto-negotiation enable 1'b0 : disable
10	SGMII_ISOLATE	1'b1 : enable SGMII software reset 1'b0 : no effect
9	SGMII_AN_RESTART	1'b1 : reset SGMII design Auto-negotiation restart (self clear) 1'b0 : no effect 1'b1 : restart auto-negotiation

00005004	PCS_DEVICE_IDENTIFIER					C45 3.3					4D544950					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_PHY_IDENTIFIER_REG3															
Type	RO															

Reset	0	1	0	0	1	1	0	1	0	1	0	1	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_PHY_IDENTIFIER_REG2															
Type	RO															
Reset	0	1	0	0	1	0	0	1	0	1	0	1	0	0	0	0

Bit(s)	Name	Description
31:16	SGMII_PHY_IDENTIFIER_REG3	Version tag of SGMII
15:0	SGMII_PHY_IDENTIFIER_REG2	Version tag of SGMII

00005008					PCS SPEED ABILITY								C45 3.5				00000001			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	SGMII_PARTNER_ABILITY_15_11					SGMII_PARTNER_ABILITY_10	SGMII_PARTNER_ABILITY_9	SGMII_PARTNER_ABILITY_8	SGMII_PARTNER_ABILITY_7	SGMII_PARTNER_ABILITY_6	SGMII_PARTNER_ABILITY_5	SGMII_PARTNER_ABILITY_4	SGMII_PARTNER_ABILITY_3	SGMII_PARTNER_ABILITY_2	SGMII_PARTNER_ABILITY_1	SGMII_PARTNER_ABILITY_0				
Type	RO					RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	SGMII_DEV_ABILITY_15	SGMII_AN_ACK	SGMII_DEV_ABILITY_13_4										SGMII_DEV_ABILITY_3	SGMII_DEV_ABILITY_2	SGMII_DEV_ABILITY_1	SGMII_DEV_ABILITY_0				
Type	RW	RO	RW										RW	RW	RW	RW				
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31:27	SGMII_PARTNER_ABILITY_15_11	link partner's advertised ability, bit 15 to 11
26	SGMII_PARTNER_ABILITY_10	link partner's advertised ability, bit 10
25	SGMII_PARTNER_ABILITY_9	link partner's advertised ability, bit 9
24	SGMII_PARTNER_ABILITY_8	link partner's advertised ability, bit 8
23	SGMII_PARTNER_ABILITY_7	link partner's advertised ability, bit 7
22	SGMII_PARTNER_ABILITY_6	link partner's advertised ability, bit 6
21	SGMII_PARTNER_ABILITY_5	link partner's advertised ability, bit 5
20	SGMII_PARTNER_ABILITY_4	link partner's advertised ability, bit 4
19	SGMII_PARTNER_ABILITY_3	link partner's advertised ability, bit 3
18	SGMII_PARTNER_ABILITY_2	link partner's advertised ability, bit 2
17	SGMII_PARTNER_ABILITY_1	link partner's advertised ability, bit 1
16	SGMII_PARTNER_ABILITY_0	link partner's advertised ability, bit 0
15	SGMII_DEV_ABILITY_15	local device's advertised ability, bit 15
14	SGMII_AN_ACK	ACK to link partner's auto-negotiation
13:4	SGMII_DEV_ABILITY_13_4	local device's advertised ability, bit 13 to 4
3	SGMII_DEV_ABILITY_3	local device's advertised ability, bit 3
2	SGMII_DEV_ABILITY_2	local device's advertised ability, bit 2

Bit(s)	Name	Description
1	SGMII_DEV_ABILITY_1	local device's advertised ability, bit 1
0	SGMII_DEV_ABILITY_0	local device's advertised ability, bit 0 (1 indicating SGMII mode)

0000500C PACKAGE_PRESENT C45 3.7 00000004

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_AN_EXPANSION_15	SGMII_AN_EXPANSION_14	SGMII_AN_EXPANSION_13	SGMII_AN_EXPANSION_12_0												
Type	RO	RO	RO	RO												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0

Bit(s)	Name	Description
15	SGMII_AN_EXPANSION_15	AN expansion register bit 15, always 0
14	SGMII_AN_EXPANSION_14	AN expansion register bit 14, always 0
13	SGMII_AN_EXPANSION_13	AN expansion register bit 13, always 0
12:0	SGMII_AN_EXPANSION_12_0	AN expansion register bit 12 to 0, bit 12 to 2 are always 11'd1, bit 1 is 0 when AN entering restart state (high priority) or is 1 when receive link partner's page cycle (medium priority) or is 0 when @SGMII_AN_EXPANSION_CLR is 1

00005010 PCS_STATUS_2 C45 3.8 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SGMII_TX_FAULT_TCH	SGMII_RX_FAULT_TCH										
Type					RO	RO										
Reset					0	0										

Bit(s)	Name	Description
11	SGMII_TX_FAULT_LATCH	indicate TXFIFO full event
10	SGMII_RX_FAULT_LATCH	indicate RXFIFO empty event

00005014 PCS_SCRATCH 00010000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_DEV_VERSION															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_SCRATCH															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	SGMII_DEV_VERSION	device version, always 16'd1
15:0	SGMII_SCRATCH	scratch register, reserved

00005018 PCS_LINK_TIMER 00098968

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name													SGMII_LINK_TIMER			
Type													RW			
Reset													1	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_LINK_TIMER															
Type	RW															
Reset	1	0	0	0	1	0	0	1	0	1	1	0	1	0	0	0

Bit(s)	Name	Description
19:0	SGMII_LINK_TIMER	Programmable link timer, delay time = SGMII_LINK_TIMER*2*(SGMII : 8ns / HSGMII : 3.2ns)

0000501C PCS_DEC_ERROR_CNT 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_DEC_ERROR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	SGMII_DEC_ERROR_CNT	decode error count, reset when @SGMII_ISOLATE=1 or @SGMII_SW_RESET=1, increase when character error or disparity error

00005020 SGMII_MODE 3112001B

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					SGMII_SEND_AN_ERROR_EN	SGMII_CODE_SYNC_SET_EN	SGMII_CODE_SYNC_SET_VAL	SGMII_REMOTE_FAULT_DIS			SGMII_IF_MODE_5_0					
Type					RW	RW	RW	RW			RW					
Reset					0	0	0	0			0	1	1	0	1	1

Bit(s)	Name	Description
11	SGMII_SEND_AN_ERROR_EN	Remote fault control during AN 1'b0 : don't send remote fault when capability is not match
10	SGMII_CODE_SYNC_SET_EN	1'b1 : send remote fault when capability is not match Manually set code_sync enable bit 1'b0 : disable
9	SGMII_CODE_SYNC_SET_VAL	1'b1 : enable Manually set code_sync value when SGMII_CODE_SYNC_SET_EN = 1 1'b0 : sync loss 1'b1 : sync acquired

Bit(s)	Name	Description
8	SGMII_REMOTE_FAULT_DIS	Update control of Remote Fault 1'b0 : tx_config_reg[13:12] = 10 when SGMII_DEV_ABILITY_13_4[9:8] is 10, tx_config_reg[13:12] = 01 when remaining in link fail state, tx_config_reg[13:12] = 11 when remaining in AN error state, and tx_config_reg[13:12] = 00 when normal state. Priority of all above states are from high to low. 1'b1 : tx_config_reg[13:12] is from SGMII_DEV_ABILITY_13_4[9:8] (sw control totally)
5:0	SGMII_IF_MODE_5_0	Interface mode [0] : need to set 1, do not change [1] : enable of advertising speed and duplex by AN [3:2] : force speed setting when [1] = 0, 2'b00 : 10Mbps / 2'b01 : 100Mbps / 2'b10 : 1Gbps / 2'b11 : reserved [4] : force duplex setting when [1] = 0, 1'b0 : full duplex / 1'b1 : half duplex [5] : reserved

00005024	SGMII_RESERVED															00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	SGMII_RESERVED_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	SGMII_RESERVED_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	SGMII_RESERVED_REG	reserved registers

0000502C	<u>SGMII_WO_REG_VALUE</u>															00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Name													SGMII_ RO_SW _RESET	SGMII_ RO_AN _RESTA RT	SGMII_ RO_AN _EXPA NSION _CLR	SGMII_ RO_LINK _RST
Type													RO	RO	RO	RO
Reset													0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
19	SGMII_RO_SW_RESET	Read only signal for debug
18	SGMII_RO_AN_RESTART	Read only signal for debug
17	SGMII_RO_AN_EXPANSION_CLR	Read only signal for debug
16	SGMII_RO_LINK_RST	Read only signal for debug

00005034 SGMII_RESERVED_0 C45 3.2001 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																SGMII_ SW_RE SET
Type																WO
Reset																0

Bit(s)	Name	Description
0	SGMII_SW_RESET	SGMII design reset
		1'b0 : no effect
		1'b1 : reset

00005040 SGMII_RW_0

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name		SGMII_PCS_DEC_ERROR_CNT_READ_LATCH														
Type		RW														
Reset		0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
30	SGMII_PCS_DEC_ERROR_CNT_READ_LATCH	Latch current decode error count to SGMII_DEC_ERROR_CNT for read
		1'b0 : no effect
		1'b1 : latch

0000504C INTERRUPT CONTROL 0 FFFF0000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INTS_MASK															
Type	RW															
Reset	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	INTS_CLEAR															
Type	WO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	INTS_MASK	Interrupt mask
		[15] : link up
		[14] : link down
		[13] : AN done

Bit(s)	Name	Description
		[12] : re AN
		[11] : tx basepage
		[10] : rx basepage
		[9] : tx nextpage
		[8] : rx nextpage
		[7] : remote fault
		[6] : coding error
		[5] : tx fifo ptr error
		[4] : rx fifo ptr error
		[3] : reserved
		[2] : reserved
		[1] : reserved
		[0] : reserved
15:0	INTS_CLEAR	Interrupt clear (self-clear)
		[15] : link up
		[14] : link down
		[13] : AN done
		[12] : re AN
		[11] : tx basepage
		[10] : rx basepage
		[9] : tx nextpage
		[8] : rx nextpage
		[7] : remote fault
		[6] : coding error
		[5] : tx fifo ptr error

Bit(s)	Name	Description
		[4] : rx fifo ptr error
		[3] : reserved
		[2] : reserved
		[1] : reserved
		[0] : reserved

00005050 INTERRUPT CONTROL 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	INTS_STATUS															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name																
Type																
Reset																

Bit(s)	Name	Description
31:16	INTS_STATUS	Interrupt Status
		[15] : link up
		[14] : link down
		[13] : AN done
		[12] : re AN
		[11] : tx basepage
		[10] : rx basepage
		[9] : tx nextpage
		[8] : rx nextpage
		[7] : remote fault
		[6] : coding error

Bit(s)	Name	Description
		[5] : tx fifo ptr error
		[4] : rx fifo ptr error
		[3] : reserved
		[2] : reserved
		[1] : reserved
		[0] : reserved

00005060	QPHY_SIG_DET_CTRL				QPHY signal detect threshold control												40120005
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	FRC_SIG_DET	SIG_DET_CR															
Type	RW	RW															
Reset	0	1															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name																	
Type																	
Reset																	

Bit(s)	Name	Description
31	FRC_SIG_DET	PCS's signal_detect input force mode
		1'b0 : disable
		1'b1 : enable
30	SIG_DET_CR	Control PCS's signal_detect input value if FRC_SIG_DET = 1
		1'b0 : signal not detected
		1'b1 : signal detected

000050C4	PAT_GEN_CTRL_0				Pattern Gen control_0												00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	UDP_DATA_15_0																			
Type	RW																			

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								BIST_ERR	BIST_RUN	BIST_OK	PRBS_INJERR	RENEW_MODE	PRBS_MODE		PRBS_CHECK	PRBS_EN
Type								RO	RO	RO	RW	RW	RW		RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:16	UDP_DATA_15_0	User define pattern [15:0]
8	BIST_ERR	BIST Error flag (error bit received)
7	BIST_RUN	BIST Run flag (Pattern generate and check period)
6	BIST_OK	BIST OK flag (no error bit received)
5	PRBS_INJERR	PRBS pattern error bits injection
		1'b0 : TX send PRBS pattern normally
		1'b1 : TX send specific pattern 20'h5a5a5
4	RENEW_MODE	Mode of Next PRBS golden pattern generation for check
		1'b0 : using first RX data to polynomial LFSR
		1'b1 : using every RX data to polynomial LFSR
3:2	PRBS_MODE	Type of pattern for generation
		2'b00 : PRBS-7
		2'b01 : User define pattern
		2'b10 : Clock pattern
		2'b11 : No used
1	PRBS_CHECK	Start to calculate PRBS error count enable
		1'b0 : no active
		1'b1 : active
0	PRBS_EN	Pattern Gen enable
		1'b0 : disable
		1'b1 : enable

000050C8	PAT_GEN_CTRL_1										Pattern Gen control_1						00000000					
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16						
Name	UDP_DATA_47_16																					
Type	RW																					

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DATA_47_16															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UDP_DATA_47_16	User define pattern [47:16]

000050CC **PAT_GEN_CTRL_2** Pattern Gen control_2 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	UDP_DATA_79_48															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	UDP_DATA_79_48															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	UDP_DATA_79_48	User define pattern [79:48]

000050D0 **PAT_GEN_CTRL_3** Pattern Gen control_3 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	BIST_ERR_CNT															
Type	RO															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	BIST_ERR_CNT	PRBS error count

000050E8 QPHY_PWR_STATE_CTRL QPHY power state control 00000010

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name												PHYA_PWD				
Type												RW				
Reset												1				

Bit(s)	Name	Description
4	PHYA_PWD	Power down SERDES totally
		1'b0 : QPHY is under power on state
		1'b1 : QPHY is under power down state

000050EC QPHY_WRAP_CTRL QPHY wrapper control 00000501

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										TBI_RX_DISABLE	TBI_TX_DISABLE	PCS_R2T_LOOPBACK	QPHY_R2T_LOOPBACK	PCS_T2R_LOOPBACK	RX_BIT_POLARITY	TX_BIT_POLARITY
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	1

Bit(s)	Name	Description
6	TBI_RX_DISABLE	TBI interface of RX data disable
		1'b0 : enable RX data
		1'b1 : disable RX data
5	TBI_TX_DISABLE	TBI interface of TX data disable

Bit(s)	Name	Description
		1'b0 : enable TX data
4	PCS_R2T_LOOPBACK	1'b1 : disable TX data PCS level RX loopback to TX enable
		1'b0 : disable
3	QPHY_R2T_LOOPBACK	1'b1 : enable PMA level RX loopback to TX enable
		1'b0 : disable
2	PCS_T2R_LOOPBACK	1'b1 : enable PCS level TX loopback to RX enable
		1'b0 : disable
1	RX_BIT_POLARITY	1'b1 : enable RX bit polarity control
		1'b0 : normal
0	TX_BIT_POLARITY	1'b1 : inversed TX bit polarity control (TX default inversed in MT7531)
		1'b0 : normal
		1'b1 : inversed

000050F0		I2C_CTRL				I2C interface control										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name															I2C_M ODE_C ODE R_CTRL _SEL	I2C_M ODE_C R_CTRL _SEL	
Type															RW	RW	
Reset															0	0	

Bit(s)	Name	Description
1	I2C_MODE	CR accessing source control when I2C_MODE_CR_CTRL_SEL = 1 1'b0 : form AXI bus 1'b1 : from external I2C
0	I2C_MODE_CR_CTRL_SEL	CR accessing source control 1'b0 : depend on test_mode by strap to decide CR access form AXI bus(0) or external I2C(1) 1'b1 : depend on I2C_MODE to decide CR access form AXI bus(0) or external I2C(1)

Module name: sgmiu_reg_phya_0 Base address: (+0x00005100)

Address	Name	Width	Register Function
00005128	OFFSETX28H	32	ANA RG_ Control Signals III

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													RG_TPHY_SPEED			
Type													RW			
Reset													0	0		

Bit(s)	Name	Description
3:2	RG_TPHY_SPEED	Speed select 2'b00: 1.25G bps (SGMII 1G) 2'b01: 3.125G bps (SGMII 2.5G)

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8 Switch System Control

8.1 Introduction

Switch system control contains PHY auto-polling (MDIO master), MDIO slave and EEPROM master. These 3 parts provide sufficient accessing ability for switch management. Additionally, it supports interrupt and PHY status for indication.

8.2 Features

- Support MDIO master with clock rate up to 25MHz
- Support MDIO slave for management
- Support external PHY auto-polling control
- Support PHY indirect access control
- Support EEPROM indirect access control
- Support interrupt control
- Support 7 port PHY status for monitor

8.3 Block Diagram

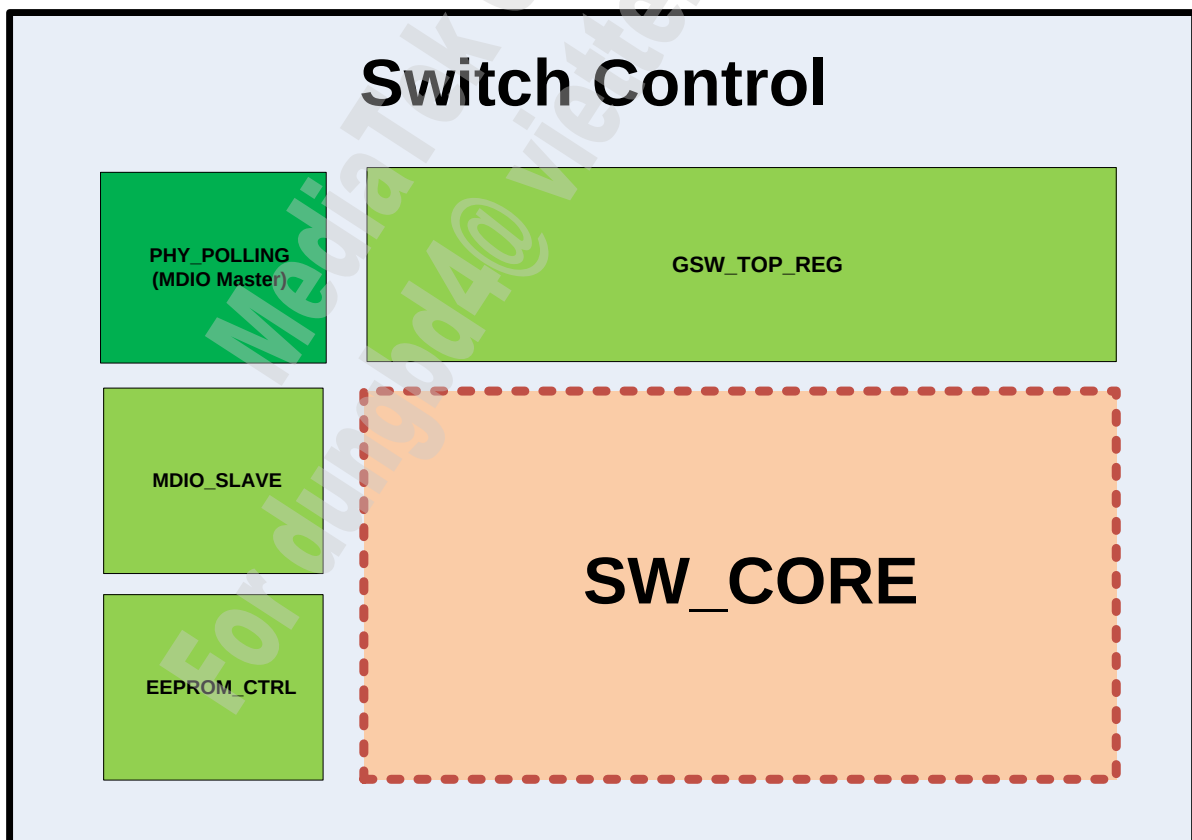


Figure 8-1. Switch system control block diagram

8.4 Theory of Operations

8.4.1 EEPROM Programming Format

The data format of the EEPROM that can be recognized by MT7531 is described in the following table. The 1st two words of this EEPROM should be Chip ID, so that the loader can identify this EEPROM. Thus, in the unit of 6 bytes, the 1st two words are the address, and rest 4 bytes are the data. To escape from the auto-loading operation, an address greater than 0x7fff is adopted.

Table 8-1. EEPROM Data Format

Address	Content	Note
0	0x75	Chip ID. Only 0x7531 can make the auto-load work.
1	0x31	
2	addr[15:8]	address[15:0]
3	addr[7:0]	
4	data[31:24]	data[31:0]
5	data[23:16]	
6	data[15:8]	
7	data[7:0]	
...	...	...
6n+2	addr[15:8]	address[15:0]
6n+3	addr[7:0]	
6n+4	data[31:24]	data[31:0]
6n+5	data[23:16]	
6n+6	data[15:8]	
6n+7	data[7:0]	
...	...	...
6m+2	escape_word[15:8]	The address[15:0] used as the escape word when it is greater than 0x07ff. If escape word is "0xfffc", EEPROM I2C master SCL/SDA pins will switch to SMI MDC/MDIO slave function after EEPROM auto-load done.
6m+3	escape_word[7:0]	

8.5 Register Definition

Module name: SYS Base address: (+0x7000)

Address	Name	Width	Register Function
00007000	<u>SYS_CTRL</u>	32	System Control
00007008	<u>SYS_INT_EN</u>	32	System Interrupt Enable
0000700C	<u>SYS_INT_STS</u>	32	System Interrupt Status
00007014	<u>PMDC_CFG</u>	32	PMDC Control Register
00007018	<u>PHY_POLL</u>	32	PHY Polling and SMI Master Control Register
0000701C	<u>PHY_IAC</u>	32	PHY Indirect Access Control
00007020	<u>PSR_P3_P0</u>	32	PHY Status Register for Port 3 ~ Port 0
00007024	<u>PSR_P6_P4</u>	32	PHY Status Register for Port 6 ~ Port 4
00007028	<u>PAUSE_CAP_P6_P0</u>	32	MAC Pause TX/RX Capability Register for Port 6 ~ Port 0
00007124	<u>EEPR_STS</u>	32	EEPROM STATUS REGISTER

00007000 SYS_CTRL System Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name										ACL_TAB_INIT	MAC_TAB_INIT	VLAN_TAB_INIT				BMU_MEM_INIT
Type										RO	RO	RO				RO
Reset										0	0	0				0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	COL_BIST_STS	TRTCM_BIST_STS	MASK_BIST_STS	CTRL_BIST_STS	ADDR_BIST_STS	VLN_BIST_STS	MIB_BIST_STS	PB_BIST_STS	PL_BIST_STS	FL_BIST_STS	MBIST_CMP	MBIST_EN			SW_SYST_RST	SW_RESET_RST
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RW			W1S	W1S
Reset	0	0	0	0	0	0	0	0	0	0	0	0			0	0

Bit(s)	Name	Description
22	ACL_TAB_INIT	ACL Table Initialization Complete
		1: Complete

Bit(s)	Name	Description
		0: Not Ready
21	MAC_TAB_INIT	MAC Table Initialization Complete 1: Complete
		0: Not Ready
20	VLAN_TAB_INIT	VLAN Table Initialization Complete 1: Complete
		0: Not Ready
16	BMU_MEM_INIT	BMU Memory Initialization Complete 1: Complete
		0: Not Ready
15	COL_BIST_STS	COL BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
14	TRTCM_BIST_STS	TRTCM BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
13	MASK_BIST_STS	Mask Memory BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
12	CTRL_BIST_STS	CTRL Memory BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
11	ADDR_BIST_STS	Address Memory BIST Status This bit is valid only when MBIST_CMP is true. 1: OK

Bit(s)	Name	Description
		0: Failed
10	VLN_BIST_STS	VLAN Memory BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
9	MIB_BIST_STS	MIB Memory BIST Status (Port0~Port6) This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
8	PB_BIST_STS	Pack Buffer Memory BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
7	PL_BIST_STS	Page Link Memory BIST Status This bit is valid only when MBIST_CMP is true. 1: OK 0: Failed
6	FL_BIST_STS	Frame Link Memory BIST Status This bit is valid only when MBIST_CMP is true 1: OK 0: Failed
5	MBIST_CMP	Memory BIST Complete 1: Complete 0: Idle or not finish yet
4	MBIST_EN	No used
1	SW_SYS_RST	Software System Reset 1: Write 1 to reset switch's states to default (excluding PHY and registers). Please note that all MACs must be forced to link-down before setting this bit. 0: Reset done/reset is inactive.

Bit(s)	Name	Description
0	SW_REG_RST	Software Register Reset 1: Write 1 to reset pbus and MDIO registers to default values. Please note that all MACs must be forced to link-down before setting this bit. 0: Reset done/reset is inactive.

00007008		SYS_INT_EN				System Interrupt Enable										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	ACL_INT_EN	ARL_SEC_TAG_INT_EN	ARL_SEC_VLAN_INT_EN	ARL_SEC_1G1X_INT_EN	ARL_PKT_BC_INT_EN	ARL_ERR_Q_INT_EN	ARL_PKT_QER_INT_EN	ARL_TBL_ERR_INT_EN	ARL_COL_FUL_INT_EN	ARL_COL_FUL_INT_EN				MIB_INT_EN	BMU_INT_EN	MAC_PKT_INT_EN	
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW				RW	RW	RW	
Reset	0	0	0	0	0	0	0	0	0	0				0	0	0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name										PHY6_L_C_INTEN	PHY5_L_C_INTEN	PHY4_L_C_INTEN	PHY3_L_C_INTEN	PHY2_L_C_INTEN	PHY1_L_C_INTEN	PHY0_L_C_INTEN	
Type										RW	RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	ACL_INT_EN	ACL Interrupt Enable 1: Enable 0: Disable
30	ARL_SEC_TAG_INT_EN	ARL Security Tag Interrupt Enable 1: Enable 0: Disable
29	ARL_SEC_VLAN_INT_EN	ARL Security VLAN Interrupt Enable 1: Enable 0: Disable
28	ARL_SEC_1G1X_INT_EN	ARL Security 1G Interrupt Enable 1: Enable

Bit(s)	Name	Description
		0: Disable
27	ARL_PKT_BC_INT_EN	ARL Broadcast Packet Drop Interrupt Enable 1: Enable
		0: Disable
26	ARL_EQ_ERR_INT_EN	ARL Enqueue Error Interrupt Enable 1: Enable
		0: Disable
25	ARL_PKT_QERR_INT_EN	ARL Packet Queue Error Interrupt Enable 1: Enable
		0: Disable
24	ARL_TBL_ERR_INT_EN	ARL Table Error Interrupt Enable 1: Enable
		0: Disable
23	ARL_COL_FULL_INT_EN	ARL Collision Pool Full Interrupt Enable 1: Enable
		0: Disable
22	ARL_COL_FULL_COL_INT_EN	ARL Collision Pool Full and Collision Detected Interrupt Enable 1: Enable
		0: Disable
18	MIB_INT_EN	MIB Interrupt Enable 1: Enable
		0: Disable
17	BMU_INT_EN	BMU Interrupt Enable 1: Enable
		0: Disable
16	MAC_PC_INT_EN	MAC/Port Controller Interrupt Enable 1: Enable
		0: Disable
6	PHY6_LC_INTE	PHY 6 Link-up Change Interrupt Enable

Bit(s)	Name	Description
		1: Enable
		0: Disable
5	PHY5_LC_INTE	PHY 5 Link-up Change Interrupt Enable
		1: Enable
		0: Disable
4	PHY4_LC_INTE	PHY 4 Link-up Change Interrupt Enable
		1: Enable
		0: Disable
3	PHY3_LC_INTE	PHY 3 Link-up Change Interrupt Enable
		1: Enable
		0: Disable
2	PHY2_LC_INTE	PHY 2 Link-up Change Interrupt Enable
		1: Enable
		0: Disable
1	PHY1_LC_INTE	PHY 1 Link-up Change Interrupt Enable
		1: Enable
		0: Disable
0	PHY0_LC_INTE	PHY 0 Link-up Change Interrupt Enable
		1: Enable
		0: Disable

0000700C		SYS_INT_STS				System Interrupt Status						00000000				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	ACL_INT	ARL_SE_C_TAG_INT	ARL_SE_C_VLA_N_INT	ARL_SE_C_IG1X_INT	ARL_PK_T_BC_INT	ARL_E_Q_ERR_INT	ARL_PK_T_QER_INT	ARL_TB_L_ERR_INT	ARL_C_OL_FUL_INT	ARL_C_OL_FUL_INT				MIB_INT	BMU_INT	MAC_P_C_INT
Type	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C	W1C				W1C	W1C	W1C
Reset	0	0	0	0	0	0	0	0	0	0				0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name										PHY6_L C_INT	PHY5_L C_INT	PHY4_L C_INT	PHY3_L C_INT	PHY2_L C_INT	PHY1_L C_INT	PHY0_L C_INT
Type										W1C	W1C	W1C	W1C	W1C	W1C	W1C
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
31	ACL_INT	ACL Interrupt Status 1: True 0: False
30	ARL_SEC_TAG_INT	ARL Security Tag Interrupt Status 1: True 0: False
29	ARL_SEC_VLAN_INT	ARL Security VLAN Interrupt Status 1: True 0: False
28	ARL_SEC_IG1X_INT	ARL Security 1G Interrupt Status 1: True 0: False
27	ARL_PKT_BC_INT	ARL Broadcast Packet Drop Interrupt Status 1: True 0: False
26	ARL_EQ_ERR_INT	ARL Enqueue Error Status 1: True 0: False
25	ARL_PKT_QERR_INT	ARL Packet Queue Error Status 1: True 0: False
24	ARL_TBL_ERR_INT	ARL Table Error Interrupt Status 1: True 0: False
23	ARL_COL_FULL_INT	ARL Collision Pool Full Interrupt Status

Bit(s)	Name	Description
		1: True
		0: False
22	ARL_COL_FULL_COL_INT	ARL Collision Pool Full and Collision Detected Interrupt Status
		1: True
		0: False
18	MIB_INT	MIB Interrupt Status
		1: True
		0: False
17	BMU_INT	BMU Interrupt Status
		1: True
		0: False
16	MAC_PC_INT	MAC/Port Controller Interrupt Status
		1: True
		0: False
6	PHY6_LC_INT	PHY 6 Link-up Change Interrupt Status
		1: True
		0: False
5	PHY5_LC_INT	PHY 5 Link-up Change Interrupt Status
		1: True
		0: False
4	PHY4_LC_INT	PHY 4 Link-up Change Interrupt Status
		1: True
		0: False
3	PHY3_LC_INT	PHY 3 Link-up Change Interrupt Status
		1: True
		0: False
2	PHY2_LC_INT	PHY 2 Link-up Change Interrupt Status
		1: True
		0: False

Bit(s)	Name	Description
1	PHY1_LC_INT	PHY 1 Link-up Change Interrupt Status 1: True 0: False
0	PHY0_LC_INT	PHY 0 Link-up Change Interrupt Status 1: True 0: False

00007014	PMDC_CFG							PMDC Control Register									00000032		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name								PMDC_CFG											
Type								RW											
Reset								0	0	0	1	1	0	0	1	0			

Bit(s)	Name	Description
8:0	PMDC_CFG	PHY MDC Clock Configuration It is used to configure the divider N for MDC clock frequency. The MDC clock is from 125MHz and is divided by N. Note: 1. MDC clock should not be over the MDC clock maximum value of PHY. 2. MDC Clock will be disabled when the setting value is equals to 0~4

00007018	<u>PHY_POLL</u>													PHY Polling and SMI Master Control Register			007F8600
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	

Name		PHY_AP_EN									EEE_POLL_EN							
Type		RW									RW							
Reset		0	0	0	0	0	0	0	0		1	1	1	1	1	1	1	1
Bit		15	14	13	12	11	10	9	8		7	6	5	4	3	2	1	0
Name	PHY_PRE_EN	RX_TAP1_CHK_OFF		PHY_END_ADDR					C45_AT_POLL_EN			PHY_ST_ADDR						
Type	RW	RW		RW					RW			RW						
Reset	1	0		0	0	1	1	0	0			0	0	0	0	0	0	0

Bit(s)	Name	Description
30:24	PHY_AP_EN	PHY Auto-Polling Enable and PHY Status Source Selection It indicates the updating PHY status by auto-polling or side-band signals. bit 24 => port 0 bit 25 => port 1 bit 30 => port 6 1: PHY status obtained by Auto-polling 0: PHY status obtained by side-band signals
22:16	EEE_POLL_EN	PHY EEE Polling Enable It indicates polling the EEE capability of each PHY. bit 16 => port 0 bit 17 => port 1 bit 22 => port 6 1: Enable 0: Disable
15	PHY_PRE_EN	PHY Preamble Enable It indicates that the SMI master will send preamble bits (32 bits) at each MDIO read/write transaction. 1: Enable 0: Disable Note: This bit will affect both PHY auto-polling mode and PHY indirect access mode.

Bit(s)	Name	Description
14	RX_TA1_CHK_OFF	Disable the checking of RX_TA1 value. 1: Do not check the value of RX_TA1 state 0: Check the value of RX_TA1. If this value is not 0, it means that there is no response from PHYs, and all rx_data are invalid.
12:8	PHY_END_ADDR	PHY Polling End Address It indicates the end address of PHY auto-polling process.
7	C45_ATPOLL_EN	Clause 45 PHY Polling Enable Enable Clause 45 auto-polling for link status only. 1: Enable (Clause 45) 0: Disable (Clause 22)
4:0	PHY_ST_ADDR	PHY Polling Start Address It indicates the start address of PHY auto-polling process and must be the first MAC's PHY address.

0000701C			PHY_IAC		PHY Indirect Access Control												00090000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16				
Name	PHY_ACS_ST		MDIO_REG_ADDR					MDIO_PHY_ADDR					MDIO_CMD		MDIO_ST					
Type	W1S		RW					RW					RW		RW					
Reset	0		0	0	0	0	0	0	0	0	0	0	1	0	0	1				
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0				
Name	MDIO_RW_DATA																			
Type	RW																			
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Bit(s)	Name	Description
31	PHY_ACS_ST	PHY Access Start Start the indirect accessing of PHY's register. When the accessing is completed, this bit will be self-cleared to 0. 1: Start 0: Idle or indirect accessing is completed

Bit(s)	Name	Description
29:25	MDIO_REG_ADDR	MDIO Reg/Dev Address Fields Configure the Register Address Field. (Clause 22) Configure the Device Address Filed (Clause 45)
24:20	MDIO_PHY_ADDR	MDIO PHY Address Field Configure the PHY address field.
19:18	MDIO_CMD	MDIO Command Field Configure the MDIO command field. 2'b00: MDIO Address (Clause 45) 2'b01: MDIO Write 2'b10: MDIO Read (or Clause 45 - Continuous Read) 2'b11: MDIO Read (Clause 45)
17:16	MDIO_ST	MDIO Start Field Configure the MDIO start field. 2'b00: Start (Clause 45) 2'b01: Start (Clause 22) Others: Reserved
15:0	MDIO_RW_DATA	MDIO Read/Write Data Field It indicates the MDIO data field for Read/Write accessing. When READ, this is used as MDIO read data (Read Only). When Write, this is used as MDIO write data (R/W).

00007020		PSR_P3_P0				PHY Status Register for Port 3 ~ Port 0										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	LP_AN_CAP_P3	PHY_EE1000_P3	PHY_EE100_P3	PHY_XF_C_P3	PHY_DUPLEX_P3	PHY_SPEED_P3		PHY_LI_NKUP_P3	LP_AN_CAP_P2	PHY_EE1000_P2	PHY_EE100_P2	PHY_XF_C_P2	PHY_DUPLEX_P2	PHY_SP_EED_P2		PHY_LI_NKUP_P2	
Type	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO		RO	
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0		0	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	

Name	LP_AN_CAP_P1	PHY_EEE1000_P1	PHY_EEE100_P1	PHY_XFC_P1	PHY_DUPLEX_P1	PHY_SPEED_P1	PHY_LINKUP_P1	LP_AN_CAP_P0	PHY_EEE1000_P0	PHY_EEE100_P0	PHY_XFC_P0	PHY_DUPLEX_P0	PHY_SPEED_P0	PHY_LINKUP_P0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	LP_AN_CAP_P3	Port 3 Link Partner Auto-Negotiation Capability 1: Link Partner supports AN 0: Link Partner does not support AN
30	PHY_EEE1000_P3	Port 3 EEE ability at 1000Base-T 1: Support EEE at 1000Base-T 0: Do not support 3000Base-T EEE
29	PHY_EEE100_P3	Port 3 EEE ability at 100Base-Tx 1: Support EEE at 100Base-Tx 0: Do not support 300Base-Tx EEE
28	PHY_XFC_P3	Port 3 MAC Flow Control Status 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
27	PHY_DUPLEX_P3	Port 3 PHY Duplex status 1: Full-duplex 0: Half-duplex
26:25	PHY_SPEED_P3	Port 3 PHY Speed Status 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
24	PHY_LINKUP_P3	Port 3 PHY Link Status 1: Link-up 0: Link-down
23	LP_AN_CAP_P2	Port 2 Link Partner Auto-Negotiation Capability

Bit(s)	Name	Description
		1: Link Partner supports AN 0: Link Partner does not support AN
22	PHY_EEE1000_P2	Port 2 EEE ability at 1000Base-T 1: Support EEE at 1000Base-T 0: Do not support 2000Base-T EEE
21	PHY_EEE100_P2	Port 2 EEE ability at 100Base-Tx 1: Support EEE at 100Base-Tx 0: Do not support 200Base-Tx EEE
20	PHY_XFC_P2	Port 2 MAC Flow Control Status 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
19	PHY_DUPLEX_P2	Port 2 PHY Duplex status 1: Full-duplex 0: Half-duplex
18	PHY_SPEED_P2	Port 2 PHY Speed Status 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
16	PHY_LINKUP_P2	Port 2 PHY Link Status 1: Link-up 0: Link-down
15	LP_AN_CAP_P1	Port 1 Link Partner Auto-Negotiation Capability 1: Link Partner supports AN 0: Link Partner does not support AN
14	PHY_EEE1000_P1	Port 1 EEE ability at 1000Base-T 1: Support EEE at 1000Base-T 0: Do not support 1000Base-T EEE
13	PHY_EEE100_P1	Port 1 EEE ability at 100Base-Tx

Bit(s)	Name	Description
		1: SupportEEE at 100Base-Tx
		0: Do not support 100Base-TxEEE
12	PHY_XFC_P1	Port 1 MAC Flow Control Status
		1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).
		0: Do not support MAC flow control
11	PHY_DUPLEX_P1	Port 1 PHY Duplex status
		1: Full-duplex
		0: Half-duplex
10:9	PHY_SPEED_P1	Port 1 PHY Speed Status
		2'b00: 10Mbps
		2'b01: 100Mbps
		2'b10: 1000Mbps
		2'b11: Reserved
8	PHY_LINKUP_P1	Port 1 PHY Link Status
		1: Link-up
		0: Link-down
7	LP_AN_CAP_P0	Port 0 Link Partner Auto-Negotiation Capability
		1: Link Partner is Auto-negotiable
		0: Link Partner is not Auto-negotiable
		Note: While PHY is link-up but LP_AN_CAP is false, it means that the current link-up state is generated by Parallel Detection. So the current phy_speed and phy_duplex bits are updated from PHY's Link Partner advertisement register (REG 05). No speed or duplex validity is guaranteed.
6	PHY_EEE1000_P0	Port 0 EEE ability at 1000Base-T
		1: SupportEEE at 1000Base-T
		0: Do not support 1000Base-TEEE
5	PHY_EEE100_P0	Port 0 EEE ability at 100Base-Tx
		1: SupportEEE at 100Base-Tx
		0: Do not support 100Base-TxEEE
4	PHY_XFC_P0	Port 0 MAC Flow Control Status

Bit(s)	Name	Description
		1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).
		0: Do not support MAC flow control
3	PHY_DUPLEX_P0	Port 0 PHY Duplex status 1: Full-duplex 0: Half-duplex
2:1	PHY_SPEED_P0	Port 0 PHY Speed Status 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
0	PHY_LINKUP_P0	Port 0 PHY Link Status 1: Link-up 0: Link-down

00007024 PSR_P6_P4 PHY Status Register for Port 6 ~ Port 4 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name									LP_AN_CAP_P6	PHY_EE1000_P6	PHY_EE100_P6	PHY_XF_C_P6	PHY_DUPLEX_P6	PHY_SPEED_P6		PHY_LINKUP_P6
Type									RO	RO	RO	RO	RO	RO		RO
Reset									0	0	0	0	0	0		0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	LP_AN_CAP_P5	PHY_EE1000_P5	PHY_EE100_P5	PHY_XF_C_P5	PHY_DUPLEX_P5	PHY_SPEED_P5		PHY_LINKUP_P5	LP_AN_CAP_P4	PHY_EE1000_P4	PHY_EE100_P4	PHY_XF_C_P4	PHY_DUPLEX_P4	PHY_SPEED_P4		PHY_LINKUP_P4
Type	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO		RO
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
23	LP_AN_CAP_P6	Port 6 Link Partner Auto-Negotiation Capability

Bit(s)	Name	Description
		1: Link Partner supports AN 0: Link Partner does not support AN
22	PHY_EEE1000_P6	Port 6 EEE ability at 1000Base-T 1: Support EEE at 1000Base-T 0: Do not support 6000Base-T EEE
21	PHY_EEE100_P6	Port 6 EEE ability at 100Base-Tx 1: Support EEE at 100Base-Tx 0: Do not support 600Base-Tx EEE
20	PHY_XFC_P6	Port 6 MAC Flow Control Status 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
19	PHY_DUPLEX_P6	Port 6 PHY Duplex status 1: Full-duplex 0: Half-duplex
18	PHY_SPEED_P6	Port 6 PHY Speed Status 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
16	PHY_LINKUP_P6	Port 6 PHY Link Status 1: Link-up 0: Link-down
15	LP_AN_CAP_P5	Port 5 Link Partner Auto-Negotiation Capability 1: Link Partner supports AN 0: Link Partner does not support AN
14	PHY_EEE1000_P5	Port 5 EEE ability at 1000Base-T 1: Support EEE at 1000Base-T 0: Do not support 5000Base-T EEE
13	PHY_EEE100_P5	Port 5 EEE ability at 100Base-Tx

Bit(s)	Name	Description
		1: Support EEE at 100Base-Tx 0: Do not support 500Base-Tx EEE
12	PHY_XFC_P5	Port 5 MAC Flow Control Status 1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames). 0: Do not support MAC flow control
11	PHY_DUPLEX_P5	Port 5 PHY Duplex status 1: Full-duplex 0: Half-duplex
10:9	PHY_SPEED_P5	Port 5 PHY Speed Status 2'b00: 10Mbps 2'b01: 100Mbps 2'b10: 1000Mbps 2'b11: Reserved
8	PHY_LINKUP_P5	Port 5 PHY Link Status 1: Link-up 0: Link-down
7	LP_AN_CAP_P4	Port 4 Link Partner Auto-Negotiation Capability 1: Link Partner is Auto-negotiable 0: Link Partner is not Auto-negotiable Note: While PHY is link-up but LP_AN_CAP is false, it means that the current link-up state is generated by Parallel Detection. So the current phy_speed and phy_duplex bits are updated from PHY's Link Partner advertisement register (REG 05). No speed or duplex validity is guaranteed.
6	PHY_EEE1000_P4	Port 4 EEE ability at 1000Base-T 1: Support EEE at 1000Base-T 0: Do not support 5000Base-T EEE
5	PHY_EEE100_P4	Port 4 EEE ability at 100Base-Tx 1: Support EEE at 100Base-Tx 0: Do not support 500Base-Tx EEE
4	PHY_XFC_P4	Port 4 MAC Flow Control Status

Bit(s)	Name	Description
		1: Support MAC Flow Control (Both local and Link Partner support MAC flow control (pause) frames).
		0: Do not support MAC flow control
3	PHY_DUPLEX_P4	Port 4 PHY Duplex status
		1: Full-duplex
		0: Half-duplex
2:1	PHY_SPEED_P4	Port 4 PHY Speed Status
		2'b00: 10Mbps
		2'b01: 100Mbps
		2'b10: 1000Mbps
		2'b11: Reserved
0	PHY_LINKUP_P4	Port 4 PHY Link Status
		1: Link-up
		0: Link-down

00007028 PAUSE_CAP_P6_P0 **MAC Pause TX/RX Capability Register for Port 6 ~ Port 0** 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			MAC_R XFC_P6	MAC_T XFC_P6	MAC_R XFC_P5	MAC_T XFC_P5	MAC_R XFC_P4	MAC_T XFC_P4	MAC_R XFC_P3	MAC_T XFC_P3	MAC_R XFC_P2	MAC_T XFC_P2	MAC_R XFC_P1	MAC_T XFC_P1	MAC_R XFC_P0	MAC_T XFC_P0
Type			RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13	MAC_RXFC_P6	Port 6 MAC Rx Pause Capability
		1: Support MAC Rx Pause Capability

Bit(s)	Name	Description
		0: Do not support MAC Rx Pause Capability
12	MAC_TXFC_P6	Port 6 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
11	MAC_RXFC_P5	Port 5 MAC Rx Pause Capability 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
10	MAC_TXFC_P5	Port 5 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
9	MAC_RXFC_P4	Port 4 MAC Rx Pause Capability 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
8	MAC_TXFC_P4	Port 4 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
7	MAC_RXFC_P3	Port 3 MAC Rx Pause Capability 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
6	MAC_TXFC_P3	Port 3 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
5	MAC_RXFC_P2	Port 2 MAC Rx Pause Capability 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
4	MAC_TXFC_P2	Port 2 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
3	MAC_RXFC_P1	Port 1 MAC Rx Pause Capability

Bit(s)	Name	Description
		1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
2	MAC_TXFC_P1	Port 1 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability
1	MAC_RXFC_P0	Port 0 MAC Rx Pause Capability 1: Support MAC Rx Pause Capability 0: Do not support MAC Rx Pause Capability
0	MAC_TXFC_P0	Port 0 MAC Tx Pause Capability 1: Support MAC Tx Pause Capability 0: Do not support MAC Tx Pause Capability

00007124		EEPR_STS				EEPROM STATUS REGISTER										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name															EP_AL_DONE_2_SMI	EP_AL_DONE	
Type															RO	RO	
Reset															0	0	

Bit(s)	Name	Description
1	EP_AL_DONE_2_SMI	After EEPROM auto-load, whether switch to SMI nor not 1: Detected ROM code command with "0xFFFF" address, EEPROM I2C master SCL/SDA pins switch to SMI MDC/MDIO slave function 0: Keeps EEPROM I2C master SCL/SDA pins
0	EP_AL_DONE	EEPROM auto-load status indicator

Bit(s)	Name	Description
		1: DONE
		0: Not yet

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9 TOP

9.1 Introduction

For top registers, the major digital items are STRAP and LED.

9.2 Block Diagram

9.2.1 STRAP

Normally, the strap values are from PAD. By setting SWSTRAP.chg_strap to 1, and its corresponding strap field in SWSTRAP, the output strap values are replaced.

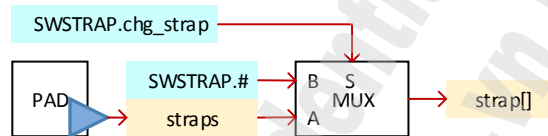


Figure 9-1 STRAP Logic

9.2.2 LED

LED_SRC is used to select the LED output source. If 0, PHYDO from GPHY are selected, else loop detection data is applied.

Also, the LED output polarity is affected by straps. If strap get 0, then the related LED output will be high active. If strap get 1, then the related LED output will be low active.

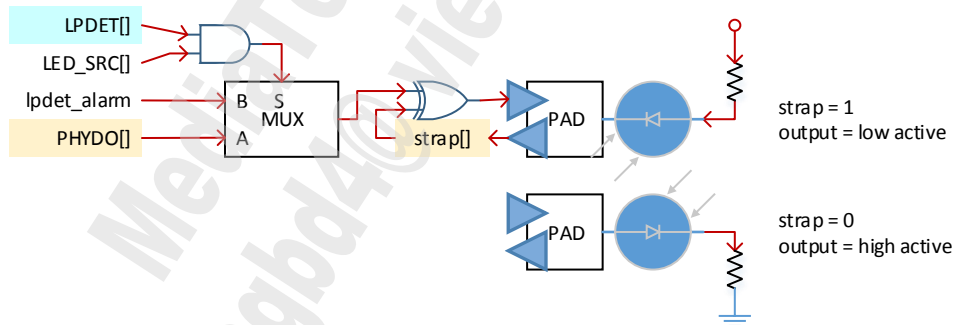


Figure 9-2 LED Logic

9.3 Register Definition

Module name: TOP Base address: (+0x7800)

Address	Name	Width	Register Function
00007800	<u>STRAP</u>	32	Strap Status Register
00007804	<u>SWSTRAP</u>	32	Software Strap Register
00007818	<u>LED_SRC</u>	32	LED Source Selection
0000781C	<u>CREV</u>	32	Chip Revision

00007800 STRAP Strap Status Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										phy_en	eep_dis			pon_lt	eep_mode	tm_dis
Type										RO	RO			RO	RO	RO
Reset										0	0			0	0	0

Bit(s)	Name	Description
6	phy_en	Embedded PHY Enable 1'b1: enable 1'b0: disable
5	eep_dis	EEPROM autoload disable 1'b1: disable 1'b0: enable
2	pon_lt	Enable Power on Light (TM_DIS=1) 1'b1: enable 1'b0: disable
1	eep_mode	EEPROM mode selection 1'b1: EEPROM size greater than 16Kb (24C32~24C256) 1'b0: EEPROM size lesser than or equal to 16Kb (24C02~24C16)
0	tm_dis	test mode strap 1'b1: disable (default) 1'b0: enable test mode

00007804 SWSTRAP Software Strap Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								chg_strap		phy_en	eeep_dis	eee_dis		pon_lt	eeep_mode	tm_dis
Type								RW		RW	RW	RW		RW	RW	RW
Reset								0		0	0	0		0	0	0

Bit(s)	Name	Description
8	chg_strap	Change STRAP setting 1'b1: Change 1'b0: Use default STRAP setting
6	phy_en	Embedded PHY Enable 1'b1: enable 1'b0: disable
5	eeep_dis	EEPROM autoload disable 1'b1: disable 1'b0: enable
4	eee_dis	EEE disable 1'b1: disable EEE 1'b0: enable EEE
2	pon_lt	Enable Power on Light (TM_DIS=1) 1'b1: enable 1'b0: disable
1	eeep_mode	EEPROM mode selection 1'b1: EEPROM size greater than 16Kb (24C32~24C256) 1'b0: EEPROM size lesser than or equal to 16Kb (24C02~24C16)
0	tm_dis	test mode strap 1'b1: disable (default) 1'b0: enable test mode

00007818

LED_SRC

LED Source Selection

00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name							P4		P3		P2		P1		P0	
Type							RW		RW		RW		RW		RW	
Reset							0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:8	P4	P4 LED Source Selection For individual LED 1'b0: P4 PHY 1'b1: Hardware Loop Detect Alarm of P4. When P4 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P4 PHY.
7:6	P3	P3 LED Source Selection For individual LED 1'b0: P3 PHY 1'b1: Hardware Loop Detect Alarm of P3. When P3 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P3 PHY.
5:4	P2	P2 LED Source Selection For individual LED 1'b0: P2 PHY 1'b1: Hardware Loop Detect Alarm of P2. When P2 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P2 PHY.
3:2	P1	P1 LED Source Selection For individual LED 1'b0: P1 PHY 1'b1: Hardware Loop Detect Alarm of P1. When P1 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P1 PHY.
1:0	P0	P0 LED Source Selection For individual LED 1'b0: P0 PHY 1'b1: Hardware Loop Detect Alarm of P0. When P0 hardware loopback is detected, this LED will flash. Otherwise, this LED is still used by P0 PHY.

0000781C CREV Chip Revision 75310001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	CHIP_NAME															
Type	RO															
Reset	0	1	1	1	0	1	0	1	0	0	1	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													CHIP_REV			
Type													RO			
Reset													0	0	0	1

Bit(s)	Name	Description
31:16	CHIP_NAME	Chip Name
3:0	CHIP_REV	Chip Revision

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10 GPIO Controller (GPIO)

10.1 Introduction

There are 27 I/O pins can be programmed as multiple purpose, including GPIO, NAND, etc. By setting up the GPIO_MODE register, specific IO is selected for specific function.

All functions should comply with the priority rule. When there are more than one IO set as the same output function, all of the selected IOs are able to output specific signals. When there are more than one IO set as the same input (or bi-directional) function, only the IO with the least GPIO index works functionally.

10.2 Features

Figure 1-1 is the block diagram of GPIO. Each GPIO controls the auxiliary mode by programming GPIO_MODE_SELx command register. GPIO_DIR, GPIO_DOUT and GPIO_PULLEN are also programmable by the same method of GPIO_MODE.

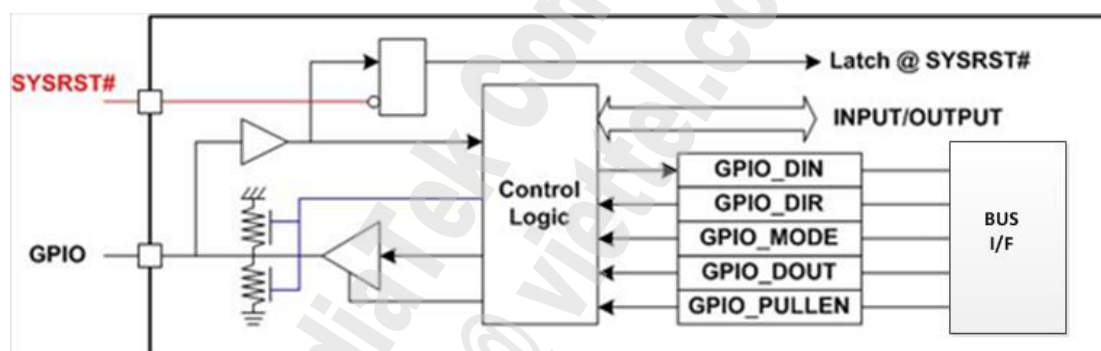


Figure 10-1. GPIO block diagram

10.3 Register Definition

Module name: GPIO Base address: (+0x0000)

Address	Name	Width	Register Function
00007C00	<u>GPIO_DIR1</u>	32	GPIO Direction Control Register 1
00007C04	<u>GPIO_DOUT1</u>	32	GPIO Data Output Register 1
00007C08	<u>GPIO_DIN1</u>	32	GPIO Data Input Register 1
00007C0C	<u>GPIO_MODE0</u>	32	GPIO Mode Control Register 0
00007C10	<u>GPIO_MODE1</u>	32	GPIO Mode Control Register 1
00007C14	<u>GPIO_MODE2</u>	32	GPIO Mode Control Register 2

00007C18	<u>GPIO_MODE3</u>	32	GPIO Mode Control Register 3
00007C1C	<u>GPIO_DBG</u>	32	GPIO Debug Register
00007C30	<u>GPIO_RSV1</u>	32	GPIO Reserve Register

00007C00 GPIO_DIR1 GPIO Direction Control Register 1 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						GPIO26_DIR_SMI_MDIO	GPIO25_DIR_SMI_MDC	GPIO24_DIR_LAN0_LED0	GPIO23_DIR_LAN0_LED1	GPIO22_DIR_LAN0_LED0	GPIO21_DIR_LAN0_LED1	GPIO20_DIR_LAN0_LED1	GPIO19_DIR_GPIO19	GPIO18_DIR_LAN2_LED0	GPIO17_DIR_LAN3_LED0	GPIO16_DIR_GPIO16
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO15_DIR_LAN3_LED1	GPIO14_DIR_LAN4_LED1	GPIO13_DIR_LAN4_LED0	GPIO12_DIR_RXD3	GPIO11_DIR_RXD2	GPIO10_DIR_RXD1	GPIO9_DIR_RG_RXD0	GPIO8_DIR_RG_RXCTL	GPIO7_DIR_RG_RXCLK	GPIO6_DIR_RG_TXCLK	GPIO5_DIR_RG_TXCTL	GPIO4_DIR_RG_TXD0	GPIO3_DIR_RG_TXD1	GPIO2_DIR_RG_TXD2	GPIO1_DIR_RG_TXD3	GPIO0_DIR_GPIO0
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
26	GPIO26_DIR_SMI_MDIO	GPIO 26 which PAD_SMI_MDIO Direction Control 0: Input 1: Output
25	GPIO25_DIR_SMI_MDC	GPIO 25 which PAD_SMI_MDC Direction Control 0: Input 1: Output
24	GPIO24_DIR_LAN0_LED0	GPIO 24 which PAD_LAN0_LED0 Direction Control 0: Input 1: Output
23	GPIO23_DIR_LAN0_LED1	GPIO 23 which PAD_LAN0_LED1 Direction Control 0: Input 1: Output

Bit(s)	Name	Description
22	GPIO22_DIR_LAN1_LED0	GPIO 22 which PAD_LAN1_LED0 Direction Control 0: Input 1: Output
21	GPIO21_DIR_LAN1_LED1	GPIO 21 which PAD_LAN1_LED1 Direction Control 0: Input 1: Output
20	GPIO20_DIR_LAN2_LED1	GPIO 20 which PAD_LAN2_LED1 Direction Control 0: Input 1: Output
19	GPIO19_DIR_GPIO_19	GPIO 19 which PAD_GPIO_19 Direction Control 0: Input 1: Output
18	GPIO18_DIR_LAN2_LED0	GPIO 18 which PAD_LAN2_LED0 Direction Control 0: Input 1: Output
17	GPIO17_DIR_LAN3_LED0	GPIO 17 which PAD_LAN3_LED0 Direction Control 0: Input 1: Output
16	GPIO16_DIR_GPIO_16	GPIO 16 which PAD_GPIO_16 Direction Control 0: Input 1: Output
15	GPIO15_DIR_LAN3_LED1	GPIO 15 which PAD_LAN3_LED1 Direction Control 0: Input 1: Output
14	GPIO14_DIR_LAN4_LED1	GPIO 14 which PAD_LAN4_LED1 Direction Control 0: Input 1: Output
13	GPIO13_DIR_LAN4_LED0	GPIO 13 which PAD_LAN4_LED0 Direction Control 0: Input

Bit(s)	Name	Description
		1: Output
12	GPIO12_DIR_RG_RXD3	GPIO 12 which PAD_RG_RXD3 Direction Control 0: Input 1: Output
11	GPIO11_DIR_RG_RXD2	GPIO 11 which PAD_RG_RXD2 Direction Control 0: Input 1: Output
10	GPIO10_DIR_RG_RXD1	GPIO 10 which PAD_RG_RXD1 Direction Control 0: Input 1: Output
9	GPIO9_DIR_RG_RXD0	GPIO 9 which PAD_RG_RXD0 Direction Control 0: Input 1: Output
8	GPIO8_DIR_RG_RXCTL	GPIO 8 which PAD_RG_RXCTL Direction Control 0: Input 1: Output
7	GPIO7_DIR_RG_RXCLK	GPIO 7 which PAD_RG_RXCLK Direction Control 0: Input 1: Output
6	GPIO6_DIR_RG_TXCLK	GPIO 6 which PAD_RG_TXCLK Direction Control 0: Input 1: Output
5	GPIO5_DIR_RG_TXCTL	GPIO 5 which PAD_RG_TXCTL Direction Control 0: Input 1: Output
4	GPIO4_DIR_RG_TXD0	GPIO 4 which PAD_RG_TXD0 Direction Control 0: Input 1: Output
3	GPIO3_DIR_RG_TXD1	GPIO 3 which PAD_RG_TXD1 Direction Control

Bit(s)	Name	Description
		0: Input
		1: Output
2	GPIO2_DIR_RG_TXD2	GPIO 2 which PAD_RG_TXD2 Direction Control
		0: Input
		1: Output
1	GPIO1_DIR_RG_TXD3	GPIO 1 which PAD_RG_TXD3 Direction Control
		0: Input
		1: Output
0	GPIO0_DIR_GPIO_0	GPIO 0 which PAD_GPIO_0 Direction Control
		0: Input
		1: Output

00007C04		GPIO_DOUT1				GPIO Data Output Register 1											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name						GPIO26_DOUT_SMI_MDIO	GPIO25_DOUT_SMI_MDC	GPIO24_DOUT_LAN0_LED0	GPIO23_DOUT_LAN0_LED1	GPIO22_DOUT_LAN1_LED0	GPIO21_DOUT_LAN1_LED1	GPIO20_DOUT_LAN2_LED1	GPIO19_DOUT_GPIO_19_LED0	GPIO18_DOUT_LAN2_LED0	GPIO17_DOUT_LAN3_LED0	GPIO16_DOUT_GPIO_16		
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset						0	0	0	0	0	0	0	0	0	0	0		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	GPIO15_DOUT_LAN3_LED1	GPIO14_DOUT_LAN4_LED1	GPIO13_DOUT_LAN4_LED0	GPIO12_DOUT_RG_R_XD3	GPIO11_DOUT_RG_R_XD2	GPIO10_DOUT_RG_R_XD1	GPIO9_DOUT_RG_RX_D0	GPIO8_DOUT_RG_RX_CTL	GPIO7_DOUT_RG_RX_CLK	GPIO6_DOUT_RG_TX_CLK	GPIO5_DOUT_RG_TX_CTL	GPIO4_DOUT_RG_TX_D0	GPIO3_DOUT_RG_TX_D1	GPIO2_DOUT_RG_TX_D2	GPIO1_DOUT_RG_TX_D3	GPIO0_DOUT_GPIO_0		
Type	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
26	GPIO26_DOUT_SMI_MDIO	GPIO 26 which PAD_SMI_MDIO Data Output Value
		0: Output 0
		1: Output 1

Bit(s)	Name	Description
25	GPIO25_DOUT_SMI_MDC	GPIO 25 which PAD_SMI_MDC Data Output Value 0: Output 0 1: Output 1
24	GPIO24_DOUT_LAN0_LED0	GPIO 24 which PAD_LAN0_LED0 Data Output Value 0: Output 0 1: Output 1
23	GPIO23_DOUT_LAN0_LED1	GPIO 23 which PAD_LAN0_LED1 Data Output Value 0: Output 0 1: Output 1
22	GPIO22_DOUT_LAN1_LED0	GPIO 22 which PAD_LAN1_LED0 Data Output Value 0: Output 0 1: Output 1
21	GPIO21_DOUT_LAN1_LED1	GPIO 21 which PAD_LAN1_LED1 Data Output Value 0: Output 0 1: Output 1
20	GPIO20_DOUT_LAN2_LED1	GPIO 20 which PAD_LAN2_LED1 Data Output Value 0: Output 0 1: Output 1
19	GPIO19_DOUT_GPIO_19	GPIO 19 which PAD_GPIO_19 Data Output Value 0: Output 0 1: Output 1
18	GPIO18_DOUT_LAN2_LED0	GPIO 18 which PAD_LAN2_LED0 Data Output Value 0: Output 0 1: Output 1
17	GPIO17_DOUT_LAN3_LED0	GPIO 17 which PAD_LAN3_LED0 Data Output Value 0: Output 0 1: Output 1
16	GPIO16_DOUT_GPIO_16	GPIO 16 which PAD_GPIO_16 Data Output Value 0: Output 0

Bit(s)	Name	Description
		1: Output 1
15	GPIO15_DOUT_LAN3_LED1	GPIO 15 which PAD_LAN3_LED1 Data Output Value
		0: Output 0
		1: Output 1
14	GPIO14_DOUT_LAN4_LED1	GPIO 14 which PAD_LAN4_LED1 Data Output Value
		0: Output 0
		1: Output 1
13	GPIO13_DOUT_LAN4_LED0	GPIO 13 which PAD_LAN4_LED0 Data Output Value
		0: Output 0
		1: Output 1
12	GPIO12_DOUT_RG_RXD3	GPIO 12 which PAD_RG_RXD3 Data Output Value
		0: Output 0
		1: Output 1
11	GPIO11_DOUT_RG_RXD2	GPIO 11 which PAD_RG_RXD2 Data Output Value
		0: Output 0
		1: Output 1
10	GPIO10_DOUT_RG_RXD1	GPIO 10 which PAD_RG_RXD1 Data Output Value
		0: Output 0
		1: Output 1
9	GPIO9_DOUT_RG_RXD0	GPIO 9 which PAD_RG_RXD0 Data Output Value
		0: Output 0
		1: Output 1
8	GPIO8_DOUT_RG_RXCTL	GPIO 8 which PAD_RG_RXCTL Data Output Value
		0: Output 0
		1: Output 1
7	GPIO7_DOUT_RG_RXCLK	GPIO 7 which PAD_RG_RXCLK Data Output Value
		0: Output 0
		1: Output 1
6	GPIO6_DOUT_RG_TXCLK	GPIO 6 which PAD_RG_TXCLK Data Output Value

Bit(s)	Name	Description
		0: Output 0
		1: Output 1
5	GPIO5_DOUT_RG_TXCTL	GPIO 5 which PAD_RG_TXCTL Data Output Value
		0: Output 0
		1: Output 1
4	GPIO4_DOUT_RG_TXD0	GPIO 4 which PAD_RG_TXD0 Data Output Value
		0: Output 0
		1: Output 1
3	GPIO3_DOUT_RG_TXD1	GPIO 3 which PAD_RG_TXD1 Data Output Value
		0: Output 0
		1: Output 1
2	GPIO2_DOUT_RG_TXD2	GPIO 2 which PAD_RG_TXD2 Data Output Value
		0: Output 0
		1: Output 1
1	GPIO1_DOUT_RG_TXD3	GPIO 1 which PAD_RG_TXD3 Data Output Value
		0: Output 0
		1: Output 1
0	GPIO0_DOUT_GPIO_0	GPIO 0 which PAD_GPIO_0 Data Output Value
		0: Output 0
		1: Output 1

00007C08	GPIO_DIN1					GPIO Data Input Register 1										0XXXXXXX
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name						GPIO26 _DIN_S MI_MD IO	GPIO25 _DIN_S MI_MD C	GPIO24 _DIN_L ANO_LE D0	GPIO23 _DIN_L ANO_LE D1	GPIO22 _DIN_L AN1_LE D0	GPIO21 _DIN_L AN1_LE D1	GPIO20 _DIN_L AN2_LE D1	GPIO19 _DIN_G PIO_19	GPIO18 _DIN_L AN2_LE D0	GPIO17 _DIN_L AN3_LE D0	GPIO16 _DIN_L GPIO_1 6
Type						RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset						X	X	X	X	X	X	X	X	X	X	X
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name	GPIO15 _DIN_L AN3_L ED1	GPIO14 _DIN_L AN4_LE D1	GPIO13 _DIN_L AN4_LE D0	GPIO12 _DIN_R G_RXD 3	GPIO11 _DIN_R G_RXD 2	GPIO10 _DIN_R G_RXD 1	GPIO9 _DIN_R G_RXD 0	GPIO8 _DIN_R G_RXC TL	GPIO7 _DIN_R G_RXC LK	GPIO6 _DIN_R G_TXCL K	GPIO5 _DIN_R G_TXC TL	GPIO4 _DIN_R G_TXD 0	GPIO3 _DIN_R G_TXD 1	GPIO2 _DIN_R G_TXD 2	GPIO1 _DIN_R G_TXD 3	GPIO0 _DIN_G PIO_0
Type	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO	RO
Reset	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Bit(s)	Name	Description
26	GPIO26_DIN_SMI_MDIO	GPIO 26 which PAD_SMI_MDIO Data Input Value
25	GPIO25_DIN_SMI_MDC	GPIO 25 which PAD_SMI_MDC Data Input Value
24	GPIO24_DIN_LAN0_LED0	GPIO 24 which PAD_LAN0_LED0 Data Input Value
23	GPIO23_DIN_LAN0_LED1	GPIO 23 which PAD_LAN0_LED1 Data Input Value
22	GPIO22_DIN_LAN1_LED0	GPIO 22 which PAD_LAN1_LED0 Data Input Value
21	GPIO21_DIN_LAN1_LED1	GPIO 21 which PAD_LAN1_LED1 Data Input Value
20	GPIO20_DIN_LAN2_LED1	GPIO 20 which PAD_LAN2_LED1 Data Input Value
19	GPIO19_DIN_GPIO_19	GPIO 19 which PAD_GPIO_19 Data Input Value
18	GPIO18_DIN_LAN2_LED0	GPIO 18 which PAD_LAN2_LED0 Data Input Value
17	GPIO17_DIN_LAN3_LED0	GPIO 17 which PAD_LAN3_LED0 Data Input Value
16	GPIO16_DIN_GPIO_16	GPIO 16 which PAD_GPIO_16 Data Input Value
15	GPIO15_DIN_LAN3_LED1	GPIO 15 which PAD_LAN3_LED1 Data Input Value
14	GPIO14_DIN_LAN4_LED1	GPIO 14 which PAD_LAN4_LED1 Data Input Value
13	GPIO13_DIN_LAN4_LED0	GPIO 13 which PAD_LAN4_LED0 Data Input Value
12	GPIO12_DIN_RG_RXD3	GPIO 12 which PAD_RG_RXD3 Data Input Value
11	GPIO11_DIN_RG_RXD2	GPIO 11 which PAD_RG_RXD2 Data Input Value
10	GPIO10_DIN_RG_RXD1	GPIO 10 which PAD_RG_RXD1 Data Input Value
9	GPIO9_DIN_RG_RXD0	GPIO 9 which PAD_RG_RXD0 Data Input Value
8	GPIO8_DIN_RG_RXCTL	GPIO 8 which PAD_RG_RXCTL Data Input Value
7	GPIO7_DIN_RG_RXCLK	GPIO 7 which PAD_RG_RXCLK Data Input Value
6	GPIO6_DIN_RG_TXCLK	GPIO 6 which PAD_RG_TXCLK Data Input Value
5	GPIO5_DIN_RG_TXCTL	GPIO 5 which PAD_RG_TXCTL Data Input Value
4	GPIO4_DIN_RG_TXD0	GPIO 4 which PAD_RG_TXD0 Data Input Value
3	GPIO3_DIN_RG_TXD1	GPIO 3 which PAD_RG_TXD1 Data Input Value
2	GPIO2_DIN_RG_TXD2	GPIO 2 which PAD_RG_TXD2 Data Input Value

Bit(s)	Name	Description
1	GPIO1_DIN_RG_TXD3	GPIO 1 which PAD_RG_TXD3 Data Input Value
0	GPIO0_DIN_GPIO_0	GPIO 0 which PAD_GPIO_0 Data Input Value

00007C0C GPIO_MODE0 GPIO Mode Control Register 0 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO7_MODE_RG_RXCLK				GPIO6_MODE_RG_TXCLK				GPIO5_MODE_RG_TXCTL				GPIO4_MODE_RG_TXD0			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO3_MODE_RG_TXD1				GPIO2_MODE_RG_TXD2				GPIO1_MODE_RG_TXD3				GPIO0_MODE_GPIO_0			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
31:28	GPIO7_MODE_RG_RXCLK	GPIO 7 which PAD_RG_RXCLK Mode Selection 0: GPIO7 (IO) 1: RG_RXCLK (IO) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B12 (IO)
27:24	GPIO6_MODE_RG_TXCLK	GPIO 6 which PAD_RG_TXCLK Mode Selection 0: GPIO6 (IO) 1: RG_TXCLK (IO) 2: Reserved 3: Reserved

Bit(s)	Name	Description
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B11 (IO)
23:20	GPIO5_MODE_RG_TXCTL	GPIO 5 which PAD_RG_TXCTL Mode Selection
		0: GPIO5 (IO)
		1: RG_TXCTL (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
19:16	GPIO4_MODE_RG_TXD0	GPIO 4 which PAD_RG_TXD0 Mode Selection
		0: GPIO4 (IO)
		1: RG_TXD0 (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
15:12	GPIO3_MODE_RG_TXD1	GPIO 3 which PAD_RG_TXD1 Mode Selection
		0: GPIO3 (IO)
		1: RG_TXD1 (IO)
		2: Reserved
		3: Reserved
		4: Reserved

Bit(s)	Name	Description
		5: Reserved
		6: Reserved
		7: Reserved
11:8	GPIO2_MODE_RG_TXD2	GPIO 2 which PAD_RG_TXD2 Mode Selection
		0: GPIO2 (IO)
		1: RG_TXD2 (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
7:4	GPIO1_MODE_RG_TXD3	GPIO 1 which PAD_RG_TXD3 Mode Selection
		0: GPIO1 (IO)
		1: RG_TXD3 (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
3:0	GPIO0_MODE_GPIO_0	GPIO 0 which PAD_GPIO_0 Mode Selection
		0: GPIO0 (IO)
		1: INTERRUPT (O)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved

Bit(s)	Name	Description
		6: Reserved
		7: DBG_MON_B18 (IO)

00007C10 GPIO_MODE1 GPIO Mode Control Register 1 11111111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO15_MODE_LAN3_LED1				GPIO14_MODE_LAN4_LED1				GPIO13_MODE_LAN4_LED0				GPIO12_MODE_RG_RXD3			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO11_MODE_RG_RXD2				GPIO10_MODE_RG_RXD1				GPIO9_MODE_RG_RXD0				GPIO8_MODE_RG_RXCTL			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
31:28	GPIO15_MODE_LAN3_LED1	GPIO 15 which PAD_LAN3_LED1 Mode Selection 0: GPIO15 (IO) 1: GPHY3_LED1_N (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B1 (IO)
27:24	GPIO14_MODE_LAN4_LED1	GPIO 14 which PAD_LAN4_LED1 Mode Selection 0: GPIO14 (IO) 1: GPHY4_LED1_N (O) 2: Reserved 3: Reserved

Bit(s)	Name	Description
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
23:20	GPIO13_MODE_LAN4_LED0	GPIO 13 which PAD_LAN4_LED0 Mode Selection
		0: GPIO13 (IO)
		1: GPHY4_LED0_N (O)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B0 (IO)
19:16	GPIO12_MODE_RG_RXD3	GPIO 12 which PAD_RG_RXD3 Mode Selection
		0: GPIO12 (IO)
		1: RG_RXD3 (IO)
		2: EXT_P_MDIO (IO)
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B17 (IO)
15:12	GPIO11_MODE_RG_RXD2	GPIO 11 which PAD_RG_RXD2 Mode Selection
		0: GPIO11 (IO)
		1: RG_RXD2 (IO)
		2: EXT_P_MDC (O)
		3: Reserved
		4: Reserved

Bit(s)	Name	Description
		5: Reserved
		6: Reserved
		7: DBG_MON_B16 (IO)
11:8	GPIO10_MODE_RG_RXD1	GPIO 10 which PAD_RG_RXD1 Mode Selection
		0: GPIO10 (IO)
		1: RG_RXD1 (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B15 (IO)
7:4	GPIO9_MODE_RG_RXD0	GPIO 9 which PAD_RG_RXD0 Mode Selection
		0: GPIO9 (IO)
		1: RG_RXD0 (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B14 (IO)
3:0	GPIO8_MODE_RG_RXCTL	GPIO 8 which PAD_RG_RXCTL Mode Selection
		0: GPIO8 (IO)
		1: RG_RXCTL (IO)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved

Bit(s)	Name	Description
		6: Reserved
		7: DBG_MON_B13 (IO)

00007C14 GPIO_MODE2 GPIO Mode Control Register 2 11110110

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO23_MODE_LAN0_LED1				GPIO22_MODE_LAN1_LED0				GPIO21_MODE_LAN1_LED1				GPIO20_MODE_LAN2_LED1			
Type	RW				RW				RW				RW			
Reset	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO19_MODE_GPIO_19				GPIO18_MODE_LAN2_LED0				GPIO17_MODE_LAN3_LED0				GPIO16_MODE_GPIO_16			
Type	RW				RW				RW				RW			
Reset	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

Bit(s)	Name	Description
31:28	GPIO23_MODE_LAN0_LED1	GPIO 23 which PAD_LAN0_LED1 Mode Selection 0: GPIO23 (IO) 1: GPHY0_LED1_N (O) 2: Reserved 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: DBG_MON_B9 (IO)
27:24	GPIO22_MODE_LAN1_LED0	GPIO 22 which PAD_LAN1_LED0 Mode Selection 0: GPIO22 (IO) 1: GPHY1_LED0_N (O) 2: Reserved 3: Reserved

Bit(s)	Name	Description
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B8 (IO)
23:20	GPIO21_MODE_LAN1_LED1	GPIO 21 which PAD_LAN1_LED1 Mode Selection
		0: GPIO21 (IO)
		1: GPHY1_LED1_N (O)
		2: EXT_P_MDIO (IO)
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B7 (IO)
19:16	GPIO20_MODE_LAN2_LED1	GPIO 20 which PAD_LAN2_LED1 Mode Selection
		0: GPIO20 (IO)
		1: GPHY2_LED1_N (O)
		2: EXT_P_MDC (O)
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B6 (IO)
15:12	GPIO19_MODE_GPIO_19	GPIO 19 which PAD_GPIO_19 Mode Selection
		0: GPIO19 (IO)
		1: Reserved
		2: Reserved
		3: Reserved
		4: Reserved

Bit(s)	Name	Description
		5: Reserved
		6: Reserved
		7: DBG_MON_B5 (IO)
11:8	GPIO18_MODE_LAN2_LED0	GPIO 18 which PAD_LAN2_LED0 Mode Selection
		0: GPIO18 (IO)
		1: GPHY2_LED0_N (O)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B4 (IO)
7:4	GPIO17_MODE_LAN3_LED0	GPIO 17 which PAD_LAN3_LED0 Mode Selection
		0: GPIO17 (IO)
		1: GPHY3_LED0_N (O)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B3 (IO)
3:0	GPIO16_MODE_GPIO_16	GPIO 16 which PAD_GPIO_16 Mode Selection
		0: GPIO16 (IO)
		1: Reserved
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved

Bit(s)	Name	Description
6:	Reserved	
7:	DBG_MON_B2 (IO)	

00007C18 GPIO_MODE3 GPIO Mode Control Register 3 00000111

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					GPIO26_MODE_SMI_MDIO				GPIO25_MODE_SMI_MDC				GPIO24_MODE_LAN0_LED0			
Type					RW				RW				RW			
Reset					0	0	0	1	0	0	0	1	0	0	0	1

Bit(s)	Name	Description
11:8	GPIO26_MODE_SMI_MDIO	GPIO 26 which PAD_SMI_MDIO Mode Selection 0: GPIO26 (IO) 1: SMI_MDIO (IO) 2: I2C_SDA (IO) 3: Reserved 4: Reserved 5: Reserved 6: Reserved 7: Reserved
7:4	GPIO25_MODE_SMI_MDC	GPIO 25 which PAD_SMI_MDC Mode Selection 0: GPIO25 (IO) 1: SMI_MDC (I) 2: I2C_SCL (O) 3: Reserved

Bit(s)	Name	Description
		4: Reserved
		5: Reserved
		6: Reserved
		7: Reserved
3:0	GPIO24_MODE_LAN0_LED0	GPIO 24 which PAD_LAN0_LED0 Mode Selection
		0: GPIO24 (IO)
		1: GPHY0_LED0_N (O)
		2: Reserved
		3: Reserved
		4: Reserved
		5: Reserved
		6: Reserved
		7: DBG_MON_B10 (IO)

00007C1C				GPIO_DBG				GPIO Debug Register								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name	DEBUG_REG																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	DEBUG_REG																		
Type	RW																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
31:0	DEBUG_REG	GPIO debug register

00007C30	GPIO_RSV1	GPIO Reserve Register	00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	GPIO_RSV1_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	GPIO_RSV1_REG															
Type	RW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31:0	GPIO_RSV1_REG	GPIO reserve register

Module name: IO_CFG_IOLT1 Base address: (+0x0000)

Address	Name	Width	Register Function
00007D00	<u>IES0_IOLT1</u>	32	GPIO GROUP IOLT1 IES0 Control
00007D04	<u>SMT0_IOLT1</u>	32	GPIO GROUP IOLT1 SMT0 Control
00007D08	<u>TDSEL0_IOLT1</u>	32	GPIO GROUP IOLT1 TDSEL0 Control
00007D0C	<u>TDSEL1_IOLT1</u>	32	GPIO GROUP IOLT1 TDSEL1 Control
00007D10	<u>RDSEL0_IOLT1</u>	32	GPIO GROUP IOLT1 RDSEL0 Control
00007D14	<u>PULLEN0_IOLT1</u>	32	GPIO GROUP IOLT1 PULLEN0 Control
00007D18	<u>PULLSEL0_IOLT1</u>	32	GPIO GROUP IOLT1 PULLSEL0 Control
00007D1C	<u>DRV0_IOLT1</u>	32	GPIO GROUP IOLT1 DRV0 Control
00007D20	<u>DRV1_IOLT1</u>	32	GPIO GROUP IOLT1 DRV1 Control

00007D00 IES0_IOLT1 GPIO GROUP IOLT1 IES0 Control 000007FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						IES_IOLT1_10_RG_RXD1	IES_IOLT1_9_RG_RXD0	IES_IOLT1_8_RG_RXCTL	IES_IOLT1_7_RG_RXCLK	IES_IOLT1_6_RG_TXCLK	IES_IOLT1_5_RG_TXCTL	IES_IOLT1_4_RG_TXD0	IES_IOLT1_3_RG_TXD1	IES_IOLT1_2_RG_TXD2	IES_IOLT1_1_RG_TXD3	IES_IOLT1_0_GPIO_0
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						1	1	1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
10	IES_IOLT1_10_RG_RXD1	RG_RXD1 IES 0: Disable 1: Enable
9	IES_IOLT1_9_RG_RXD0	RG_RXD0 IES 0: Disable 1: Enable
8	IES_IOLT1_8_RG_RXCTL	RG_RXCTL IES 0: Disable 1: Enable
7	IES_IOLT1_7_RG_RXCLK	RG_RXCLK IES 0: Disable 1: Enable
6	IES_IOLT1_6_RG_TXCLK	RG_TXCLK IES 0: Disable 1: Enable
5	IES_IOLT1_5_RG_TXCTL	RG_TXCTL IES 0: Disable

Bit(s)	Name	Description
		1: Enable
4	IES_IOLT1_4_RG_TXD0	RG_TXD0 IES 0: Disable 1: Enable
3	IES_IOLT1_3_RG_TXD1	RG_TXD1 IES 0: Disable 1: Enable
2	IES_IOLT1_2_RG_TXD2	RG_TXD2 IES 0: Disable 1: Enable
1	IES_IOLT1_1_RG_TXD3	RG_TXD3 IES 0: Disable 1: Enable
0	IES_IOLT1_0_GPIO_0	GPIO_0 IES 0: Disable 1: Enable

00007D04 SMT0 IOLT1				GPIO GROUP IOLT1 SMT0 Control												00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name						SMT_I OLT1_1 0_RG_ RXD1	SMT_I OLT1_9 _RG_R XD0	SMT_I OLT1_8 _RG_R XCTL	SMT_I OLT1_7 _RG_R XCLK	SMT_I OLT1_6 _RG_T XCLK	SMT_I OLT1_5 _RG_T XCTL	SMT_I OLT1_4 _RG_T XD0	SMT_I OLT1_3 _RG_T XD1	SMT_I OLT1_2 _RG_T XD2	SMT_I OLT1_1 _RG_T XD3	SMT_I OLT1_0 _GPIO_ 0
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	SMT_IOLT1_10_RG_RXD1	RG_RXD1 SMT 0: Disable 1: Enable
9	SMT_IOLT1_9_RG_RXD0	RG_RXD0 SMT 0: Disable 1: Enable
8	SMT_IOLT1_8_RG_RXCTL	RG_RXCTL SMT 0: Disable 1: Enable
7	SMT_IOLT1_7_RG_RXCLK	RG_RXCLK SMT 0: Disable 1: Enable
6	SMT_IOLT1_6_RG_TXCLK	RG_TXCLK SMT 0: Disable 1: Enable
5	SMT_IOLT1_5_RG_TXCTL	RG_TXCTL SMT 0: Disable 1: Enable

Bit(s)	Name	Description
4	SMT_IOLT1_4_RG_TXD0	RG_TXD0 SMT 0: Disable 1: Enable
3	SMT_IOLT1_3_RG_TXD1	RG_TXD1 SMT 0: Disable 1: Enable
2	SMT_IOLT1_2_RG_TXD2	RG_TXD2 SMT 0: Disable 1: Enable
1	SMT_IOLT1_1_RG_TXD3	RG_TXD3 SMT 0: Disable 1: Enable
0	SMT_IOLT1_0_GPIO_0	GPIO_0 SMT 0: Disable 1: Enable

00007D08	TDSEL0_IOLT1				GPIO GROUP IOLT1 TDSEL0 Control								AAAAAAAA			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDSEL_IOLT1_7_RG_RXCLK				TDSEL_IOLT1_6_RG_TXCLK				TDSEL_IOLT1_5_RG_TXCTL				TDSEL_IOLT1_4_RG_TXD0			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL_IOLT1_3_RG_TXD1				TDSEL_IOLT1_2_RG_TXD2				TDSEL_IOLT1_1_RG_TXD3				TDSEL_IOLT1_0_GPIO_0			
Type	RW				RW				RW				RW			

Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	TDSEL_IOLT1_7_RG_RXCLK	RG_RXCLK TDSEL
27:24	TDSEL_IOLT1_6_RG_TXCLK	RG_TXCLK TDSEL
23:20	TDSEL_IOLT1_5_RG_TXCTL	RG_TXCTL TDSEL
19:16	TDSEL_IOLT1_4_RG_TXD0	RG_TXD0 TDSEL
15:12	TDSEL_IOLT1_3_RG_TXD1	RG_TXD1 TDSEL
11:8	TDSEL_IOLT1_2_RG_TXD2	RG_TXD2 TDSEL
7:4	TDSEL_IOLT1_1_RG_TXD3	RG_TXD3 TDSEL
3:0	TDSEL_IOLT1_0_GPIO_0	GPIO_0 TDSEL

00007D0C				TDSEL1 IOLT1 GPIO GROUP IOLT1 TDSEL1 Control												00000AAA
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name					TDSEL_IOLT1_10_RG_RXD1				TDSEL_IOLT1_9_RG_RXD0				TDSEL_IOLT1_8_RG_RXCTL			
Type					RW				RW				RW			
Reset					1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
11:8	TDSEL_IOLT1_10_RG_RXD1	RG_RXD1 TDSEL
7:4	TDSEL_IOLT1_9_RG_RXD0	RG_RXD0 TDSEL
3:0	TDSEL_IOLT1_8_RG_RXCTL	RG_RXCTL TDSEL

00007D10 RDSEL0_IOLT1 GPIO GROUP IOLT1 RDSEL0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name											RDSEL_IOLT1_10_RG_RXD1	RDSEL_IOLT1_9_RG_RXD0	RDSEL_IOLT1_8_RG_RXCTL			
Type											RW	RW	RW			
Reset											0	0	0	0	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSEL_IOLT1_7_RG_RXCLK	RDSEL_IOLT1_6_RG_TXCLK	RDSEL_IOLT1_5_RG_TXCTL	RDSEL_IOLT1_4_RG_TXD0	RDSEL_IOLT1_3_RG_TXD1	RDSEL_IOLT1_2_RG_TXD2	RDSEL_IOLT1_1_RG_TXD3	RDSEL_IOLT1_0_GPIO_0								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
21:20	RDSEL_IOLT1_10_RG_RXD1	RG_RXD1 RDSEL
19:18	RDSEL_IOLT1_9_RG_RXD0	RG_RXD0 RDSEL
17:16	RDSEL_IOLT1_8_RG_RXCTL	RG_RXCTL RDSEL
15:14	RDSEL_IOLT1_7_RG_RXCLK	RG_RXCLK RDSEL
13:12	RDSEL_IOLT1_6_RG_TXCLK	RG_TXCLK RDSEL

Bit(s)	Name	Description
11:10	RDSEL_IOLT1_5_RG_TXCTL	RG_TXCTL RDSEL
9:8	RDSEL_IOLT1_4_RG_TXD0	RG_TXD0 RDSEL
7:6	RDSEL_IOLT1_3_RG_TXD1	RG_TXD1 RDSEL
5:4	RDSEL_IOLT1_2_RG_TXD2	RG_TXD2 RDSEL
3:2	RDSEL_IOLT1_1_RG_TXD3	RG_TXD3 RDSEL
1:0	RDSEL_IOLT1_0_GPIO_0	GPIO_0 RDSEL

00007D14		PULLEN0_IOLT1					GPIO GROUP IOLT1 PULLEN0 Control										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name						PULLEN_IOLT1_10_RG_RXD1	PULLEN_IOLT1_9_RG_RXD0	PULLEN_IOLT1_8_RG_RXCTL	PULLEN_IOLT1_7_RG_RXCLK	PULLEN_IOLT1_6_RG_TXCLK	PULLEN_IOLT1_5_RG_TXCTL	PULLEN_IOLT1_4_RG_TXD0	PULLEN_IOLT1_3_RG_TXD1	PULLEN_IOLT1_2_RG_TXD2	PULLEN_IOLT1_1_RG_TXD3	PULLEN_IOLT1_0_GPIO_0		
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		
Reset						0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
10	PULLEN_IOLT1_10_RG_RXD1	RG_RXD1 PULLEN 0:Disable pull control

Bit(s)	Name	Description
		1:Enable pull control
9	PULLEN_IOLT1_9_RG_RXD0	RG_RXD0 PULLEN 0:Disable pull control 1:Enable pull control
8	PULLEN_IOLT1_8_RG_RXCTL	RG_RXCTL PULLEN 0:Disable pull control 1:Enable pull control
7	PULLEN_IOLT1_7_RG_RXCLK	RG_RXCLK PULLEN 0:Disable pull control 1:Enable pull control
6	PULLEN_IOLT1_6_RG_TXCLK	RG_TXCLK PULLEN 0:Disable pull control 1:Enable pull control
5	PULLEN_IOLT1_5_RG_TXCTL	RG_TXCTL PULLEN 0:Disable pull control 1:Enable pull control
4	PULLEN_IOLT1_4_RG_TXD0	RG_TXD0 PULLEN 0:Disable pull control 1:Enable pull control
3	PULLEN_IOLT1_3_RG_TXD1	RG_TXD1 PULLEN 0:Disable pull control 1:Enable pull control

Bit(s)	Name	Description
2	PULLEN_IOLT1_2_RG_TXD2	RG_TXD2 PULLEN 0:Disable pull control 1:Enable pull control
1	PULLEN_IOLT1_1_RG_TXD3	RG_TXD3 PULLEN 0:Disable pull control 1:Enable pull control
0	PULLEN_IOLT1_0_GPIO_0	GPIO_0 PULLEN 0:Disable pull control 1:Enable pull control

00007D18 PULLSEL0_IOLT1 GPIO GROUP IOLT1 PULLSEL0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name						PULLSEL_IOLT1_10_RG_RXD1	PULLSEL_IOLT1_9_RG_RXD1	PULLSEL_IOLT1_8_RG_RXC1	PULLSEL_IOLT1_7_RG_RXC1	PULLSEL_IOLT1_6_RG_TXCL1	PULLSEL_IOLT1_5_RG_TXC1	PULLSEL_IOLT1_4_RG_TXD1	PULLSEL_IOLT1_3_RG_TXD1	PULLSEL_IOLT1_2_RG_TXD1	PULLSEL_IOLT1_1_RG_TXD1	PULLSEL_IOLT1_0_GPIO_0
Type						RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset						0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
10	PULLSEL_IOLT1_10_RG_RXD1	RG_RXD1 PULLSEL 0:Pull down select

Bit(s)	Name	Description
		1:Pull up select
9	PULLSEL_IOLT1_9_RG_RXD0	RG_RXD0 PULLSEL 0:Pull down select 1:Pull up select
8	PULLSEL_IOLT1_8_RG_RXCTL	RG_RXCTL PULLSEL 0:Pull down select 1:Pull up select
7	PULLSEL_IOLT1_7_RG_RXCLK	RG_RXCLK PULLSEL 0:Pull down select 1:Pull up select
6	PULLSEL_IOLT1_6_RG_TXCLK	RG_TXCLK PULLSEL 0:Pull down select 1:Pull up select
5	PULLSEL_IOLT1_5_RG_TXCTL	RG_TXCTL PULLSEL 0:Pull down select 1:Pull up select
4	PULLSEL_IOLT1_4_RG_TXD0	RG_TXD0 PULLSEL 0:Pull down select 1:Pull up select
3	PULLSEL_IOLT1_3_RG_TXD1	RG_TXD1 PULLSEL 0:Pull down select 1:Pull up select

Bit(s)	Name	Description
2	PULLSEL_IOLT1_2_RG_TXD2	RG_TXD2 PULLSEL 0:Pull down select 1:Pull up select
1	PULLSEL_IOLT1_1_RG_TXD3	RG_TXD3 PULLSEL 0:Pull down select 1:Pull up select
0	PULLSEL_IOLT1_0_GPIO_0	GPIO_0 PULLSEL 0:Pull down select 1:Pull up select

00007D1C **DRV0_IOLT1** **GPIO GROUP IOLT1 DRV0 Control** 44444442

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV_IOLT1_7_RG_RXCLK				DRV_IOLT1_6_RG_TXCLK				DRV_IOLT1_5_RG_TXCTL				DRV_IOLT1_4_RG_TXD0			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV_IOLT1_3_RG_TXD1				DRV_IOLT1_2_RG_TXD2				DRV_IOLT1_1_RG_TXD3				DRV_IOLT1_0_GPIO_0			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	1	0	0	0	1	0	0	0	0	1	0

Bit(s)	Name	Description
31:28	DRV_IOLT1_7_RG_RXCLK	RG_RXCLK DRV
27:24	DRV_IOLT1_6_RG_TXCLK	RG_TXCLK DRV
23:20	DRV_IOLT1_5_RG_TXCTL	RG_TXCTL

Bit(s)	Name	Description
		DRV
19:16	DRV_IOLT1_4_RG_TXD0	RG_TXD0
		DRV
15:12	DRV_IOLT1_3_RG_TXD1	RG_TXD1
		DRV
11:8	DRV_IOLT1_2_RG_TXD2	RG_TXD2
		DRV
7:4	DRV_IOLT1_1_RG_TXD3	RG_TXD3
		DRV
3:0	DRV_IOLT1_0_GPIO_0	GPIO_0
		DRV

00007D20		DRV1_IOLT1				GPIO GROUP IOLT1 DRV1 Control												00000444			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16					
Name																					
Type																					
Reset																					
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0					
Name					DRV_IOLT1_10_RG_RXD1				DRV_IOLT1_9_RG_RXD0				DRV_IOLT1_8_RG_RXCTL								
Type					RW				RW				RW								
Reset					0	1	0	0	0	1	0	0	0	1	0	0					

Bit(s)	Name	Description
11:8	DRV_IOLT1_10_RG_RXD1	RG_RXD1
		DRV
7:4	DRV_IOLT1_9_RG_RXD0	RG_RXD0
		DRV
3:0	DRV_IOLT1_8_RG_RXCTL	RG_RXCTL
		DRV

Bit(s)	Name	Description

Module name: IO_CFG_IOLT2 Base address: (+0x0000)

Address	Name	Width	Register Function
00007E00	<u>IES0_IOLT2</u>	32	GPIO GROUP IOLT2 IES0 Control
00007E04	<u>SMT0_IOLT2</u>	32	GPIO GROUP IOLT2 SMT0 Control
00007E08	<u>TDSEL0_IOLT2</u>	32	GPIO GROUP IOLT2 TDSEL0 Control
00007E0C	<u>TDSEL1_IOLT2</u>	32	GPIO GROUP IOLT2 TDSEL1 Control
00007E10	<u>RDSEL0_IOLT2</u>	32	GPIO GROUP IOLT2 RDSEL0 Control
00007E14	<u>PULLEN0_IOLT2</u>	32	GPIO GROUP IOLT2 PULLEN0 Control
00007E18	<u>PULLSEL0_IOLT2</u>	32	GPIO GROUP IOLT2 PULLSEL0 Control
00007E1C	<u>DRV0_IOLT2</u>	32	GPIO GROUP IOLT2 DRV0 Control
00007E20	<u>DRV1_IOLT2</u>	32	GPIO GROUP IOLT2 DRV1 Control

00007E00 IES0_IOLT2 GPIO GROUP IOLT2 IES0 Control 000001FF

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								IES_IOLT2_8_GPIO_19	IES_IOLT2_7_LAN2_LE_D0	IES_IOLT2_6_LAN3_LE_D0	IES_IOLT2_5_GPIO_16	IES_IOLT2_4_LAN3_LE_D1	IES_IOLT2_3_LAN4_LE_D1	IES_IOLT2_2_LAN4_LE_D0	IES_IOLT2_1_RXD3	IES_IOLT2_0_RXD2
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								1	1	1	1	1	1	1	1	1

Bit(s)	Name	Description
8	IES_IOLT2_8_GPIO_19	GPIO_19
		IES

Bit(s)	Name	Description
		0: Disable
		1: Enable
7	IES_IOLT2_7_LAN2_LED0	LAN2_LED0
		IES
		0: Disable
		1: Enable
6	IES_IOLT2_6_LAN3_LED0	LAN3_LED0
		IES
		0: Disable
		1: Enable
5	IES_IOLT2_5_GPIO_16	GPIO_16
		IES
		0: Disable
		1: Enable
4	IES_IOLT2_4_LAN3_LED1	LAN3_LED1
		IES
		0: Disable
		1: Enable
3	IES_IOLT2_3_LAN4_LED1	LAN4_LED1
		IES
		0: Disable
		1: Enable
2	IES_IOLT2_2_LAN4_LED0	LAN4_LED0
		IES
		0: Disable
		1: Enable
1	IES_IOLT2_1_RG_RXD3	RG_RXD3
		IES
		0: Disable

Bit(s)	Name	Description
		1: Enable
0	IES_IOLT2_0_RG_RXD2	RG_RXD2
		IES
		0: Disable
		1: Enable

00007E04				SMT0_IOLT2				GPIO GROUP IOLT2 SMT0 Control								00000000			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name								SMT_I OLT2_8 GPIO_19	SMT_I OLT2_7 LAN2_LED0	SMT_I OLT2_6 LAN3_LED0	SMT_I OLT2_5 GPIO_16	SMT_I OLT2_4 LAN3_LED1	SMT_I OLT2_3 LAN4_LED1	SMT_I OLT2_2 LAN4_LED0	SMT_I OLT2_1 RG_RXD3	SMT_I OLT2_0 RG_RXD2			
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW			
Reset								0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
8	SMT_IOLT2_8_GPIO_19	GPIO_19
		SMT
		0: Disable
		1: Enable
7	SMT_IOLT2_7_LAN2_LED0	LAN2_LED0
		SMT
		0: Disable
		1: Enable
6	SMT_IOLT2_6_LAN3_LED0	LAN3_LED0
		SMT

Bit(s)	Name	Description
		0: Disable
		1: Enable
5	SMT_IOLT2_5_GPIO_16	GPIO_16
		SMT
		0: Disable
		1: Enable
4	SMT_IOLT2_4_LAN3_LED1	LAN3_LED1
		SMT
		0: Disable
		1: Enable
3	SMT_IOLT2_3_LAN4_LED1	LAN4_LED1
		SMT
		0: Disable
		1: Enable
2	SMT_IOLT2_2_LAN4_LED0	LAN4_LED0
		SMT
		0: Disable
		1: Enable
1	SMT_IOLT2_1_RG_RXD3	RG_RXD3
		SMT
		0: Disable
		1: Enable
0	SMT_IOLT2_0_RG_RXD2	RG_RXD2
		SMT
		0: Disable
		1: Enable

00007E08

TDSEL0_IOLT2

GPIO GROUP IOLT2 TDSEL0 Control

AAAAAAAA

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	TDSEL_IOLT2_7_LAN2_LED0				TDSEL_IOLT2_6_LAN3_LED0				TDSEL_IOLT2_5_GPIO_16				TDSEL_IOLT2_4_LAN3_LED1			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL_IOLT2_3_LAN4_LED1				TDSEL_IOLT2_2_LAN4_LED0				TDSEL_IOLT2_1_RG_RXD3				TDSEL_IOLT2_0_RG_RXD2			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
31:28	TDSEL_IOLT2_7_LAN2_LED0	LAN2_LED0 TDSEL
27:24	TDSEL_IOLT2_6_LAN3_LED0	LAN3_LED0 TDSEL
23:20	TDSEL_IOLT2_5_GPIO_16	GPIO_16 TDSEL
19:16	TDSEL_IOLT2_4_LAN3_LED1	LAN3_LED1 TDSEL
15:12	TDSEL_IOLT2_3_LAN4_LED1	LAN4_LED1 TDSEL
11:8	TDSEL_IOLT2_2_LAN4_LED0	LAN4_LED0 TDSEL
7:4	TDSEL_IOLT2_1_RG_RXD3	RG_RXD3 TDSEL
3:0	TDSEL_IOLT2_0_RG_RXD2	RG_RXD2 TDSEL

00007E0C	TDSEL1_IOLT2				GPIO GROUP IOLT2 TDSEL1 Control								0000000A			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name													TDSEL_IOLT2_8_GPIO_19			
Type													RW			
Reset													1	0	1	0

Bit(s)	Name	Description
3:0	TDSEL_IOLT2_8_GPIO_19	GPIO_19
		TDSEL

00007E10 RDSEL0_IOLT2 GPIO GROUP IOLT2 RDSEL0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name															RDSEL_IOLT2_8_GPIO_19	
Type															RW	
Reset															0	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	RDSEL_IOLT2_7_LAN2_LED0	RDSEL_IOLT2_6_LAN3_LED0	RDSEL_IOLT2_5_GPIO_16	RDSEL_IOLT2_4_LAN3_LED1	RDSEL_IOLT2_3_LAN4_LED1	RDSEL_IOLT2_2_LAN4_LED0	RDSEL_IOLT2_1_RG_RXD3	RDSEL_IOLT2_0_RG_RXD2								
Type	RW	RW	RW	RW	RW	RW	RW	RW								
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
17:16	RDSEL_IOLT2_8_GPIO_19	GPIO_19
		RDSEL
15:14	RDSEL_IOLT2_7_LAN2_LED0	LAN2_LED0
		RDSEL
13:12	RDSEL_IOLT2_6_LAN3_LED0	LAN3_LED0
		RDSEL
11:10	RDSEL_IOLT2_5_GPIO_16	GPIO_16

Bit(s)	Name	Description
		RDSEL
9:8	RDSEL_IOLT2_4_LAN3_LED1	LAN3_LED1
		RDSEL
7:6	RDSEL_IOLT2_3_LAN4_LED1	LAN4_LED1
		RDSEL
5:4	RDSEL_IOLT2_2_LAN4_LED0	LAN4_LED0
		RDSEL
3:2	RDSEL_IOLT2_1_RG_RXD3	RG_RXD3
		RDSEL
1:0	RDSEL_IOLT2_0_RG_RXD2	RG_RXD2
		RDSEL

00007E14 PULLEN0_IOLT2 GPIO GROUP IOLT2 PULLEN0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	PULLEN_IOLT2_31_MCM_SMI_EN	PULLEN_IOLT2_30_DUAL_SGMII_EN														
Type	RW	RW														
Reset	0	0														
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name								PULLEN_IOLT2_8_GPIO_19	PULLEN_IOLT2_7_LAN2_LED0	PULLEN_IOLT2_6_LAN3_LED0	PULLEN_IOLT2_5_GPIO_16	PULLEN_IOLT2_4_LAN3_LED1	PULLEN_IOLT2_3_LAN4_LED1	PULLEN_IOLT2_2_LAN4_LED0	PULLEN_IOLT2_1_RG_RXD3	PULLEN_IOLT2_0_RG_RXD2
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW
Reset								0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
31	PULLEN_IOLT2_31_MCM_SMI_EN	MCM_SMI_EN
		PULLEN

Bit(s)	Name	Description
		0:Disable pull control
		1:Enable pull control
30	PULLEN_IOLT2_30_DUAL_SGMII_EN	DUAL_SGMII_EN PULLEN 0:Disable pull control 1:Enable pull control
8	PULLEN_IOLT2_8_GPIO_19	GPIO_19 PULLEN 0:Disable pull control 1:Enable pull control
7	PULLEN_IOLT2_7_LAN2_LED0	LAN2_LED0 PULLEN 0:Disable pull control 1:Enable pull control
6	PULLEN_IOLT2_6_LAN3_LED0	LAN3_LED0 PULLEN 0:Disable pull control 1:Enable pull control
5	PULLEN_IOLT2_5_GPIO_16	GPIO_16 PULLEN 0:Disable pull control 1:Enable pull control
4	PULLEN_IOLT2_4_LAN3_LED1	LAN3_LED1 PULLEN 0:Disable pull control 1:Enable pull control
3	PULLEN_IOLT2_3_LAN4_LED1	LAN4_LED1 PULLEN 0:Disable pull control

Bit(s)	Name	Description
		1:Enable pull control
2	PULLEN_IOLT2_2_LAN4_LED0	LAN4_LED0 PULLEN 0:Disable pull control 1:Enable pull control
1	PULLEN_IOLT2_1_RG_RXD3	RG_RXD3 PULLEN 0:Disable pull control 1:Enable pull control
0	PULLEN_IOLT2_0_RG_RXD2	RG_RXD2 PULLEN 0:Disable pull control 1:Enable pull control

00007E18		PULLSEL0_IOLT2				GPIO GROUP IOLT2 PULLSEL0 Control										00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name	PULLSE L_IOLT 2_31_ MCM_ SMI_E N	PULLSE L_IOLT 2_30_D UAL_S GMII_E N															
Type	RW	RW															
Reset	0	0															
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name								PULLSE L_IOLT 2_8_GP IO_19	PULLSE L_IOLT 2_7_LA N2_LE D0	PULLSE L_IOLT 2_6_LA N3_LE D0	PULLSE L_IOLT 2_5_GP IO_16	PULLSE L_IOLT 2_4_LA N3_LE D1	PULLSE L_IOLT 2_3_LA N4_LE D1	PULLSE L_IOLT 2_2_LA N4_LE D0	PULLSE L_IOLT 2_1_R G_RXD 3	PULLSE L_IOLT 2_0_R G_RXD 2	
Type								RW	RW	RW	RW	RW	RW	RW	RW	RW	
Reset								0	0	0	0	0	0	0	0	0	

Bit(s)	Name	Description
31	PULLSEL_IOLT2_31_MCM_SMI_EN	MCM_SMI_EN PULLSEL 0:Pull down select 1:Pull up select
30	PULLSEL_IOLT2_30_DUAL_SGMII_EN	DUAL_SGMII_EN PULLSEL 0:Pull down select 1:Pull up select
8	PULLSEL_IOLT2_8_GPIO_19	GPIO_19 PULLSEL 0:Pull down select 1:Pull up select
7	PULLSEL_IOLT2_7_LAN2_LED0	LAN2_LED0 PULLSEL 0:Pull down select 1:Pull up select
6	PULLSEL_IOLT2_6_LAN3_LED0	LAN3_LED0 PULLSEL 0:Pull down select 1:Pull up select
5	PULLSEL_IOLT2_5_GPIO_16	GPIO_16 PULLSEL 0:Pull down select 1:Pull up select
4	PULLSEL_IOLT2_4_LAN3_LED1	LAN3_LED1 PULLSEL 0:Pull down select 1:Pull up select
3	PULLSEL_IOLT2_3_LAN4_LED1	LAN4_LED1

Bit(s)	Name	Description
		PULLSEL
		0:Pull down select
		1:Pull up select
2	PULLSEL_IOLT2_2_LAN4_LED0	LAN4_LED0
		PULLSEL
		0:Pull down select
		1:Pull up select
1	PULLSEL_IOLT2_1_RG_RXD3	RG_RXD3
		PULLSEL
		0:Pull down select
		1:Pull up select
0	PULLSEL_IOLT2_0_RG_RXD2	RG_RXD2
		PULLSEL
		0:Pull down select
		1:Pull up select

00007E1C				GPIO GROUP IOLT2 DRV0 Control								22224244				
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name	DRV_IOLT2_7_LAN2_LED0				DRV_IOLT2_6_LAN3_LED0				DRV_IOLT2_5_GPIO_16				DRV_IOLT2_4_LAN3_LED1			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV_IOLT2_3_LAN4_LED1				DRV_IOLT2_2_LAN4_LED0				DRV_IOLT2_1_RG_RXD3				DRV_IOLT2_0_RG_RXD2			
Type	RW				RW				RW				RW			
Reset	0	1	0	0	0	0	1	0	0	1	0	0	0	1	0	0

Bit(s)	Name	Description
31:28	DRV_IOLT2_7_LAN2_LED0	LAN2_LED0
		DRV

Bit(s)	Name	Description
27:24	DRV_IOLT2_6_LAN3_LED0	LAN3_LED0 DRV
23:20	DRV_IOLT2_5_GPIO_16	GPIO_16 DRV
19:16	DRV_IOLT2_4_LAN3_LED1	LAN3_LED1 DRV
15:12	DRV_IOLT2_3_LAN4_LED1	LAN4_LED1 DRV
11:8	DRV_IOLT2_2_LAN4_LED0	LAN4_LED0 DRV
7:4	DRV_IOLT2_1_RG_RXD3	RG_RXD3 DRV
3:0	DRV_IOLT2_0_RG_RXD2	RG_RXD2 DRV

00007E20				GPIO GROUP IOLT2 DRV1 Control												00000002			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name													DRV_IOLT2_8_GPIO_19						
Type													RW						
Reset													0	0	1	0			

Bit(s)	Name	Description
3:0	DRV_IOLT2_8_GPIO_19	GPIO_19 DRV

Module name: IO_CFG_IOLB Base address: (+0x0000)

Address	Name	Width	Register Function
00007F00	<u>IES0_IOLB</u>	32	GPIO GROUP IOLB IES0 Control
00007F04	<u>SMT0_IOLB</u>	32	GPIO GROUP IOLB SMT0 Control
00007F08	<u>TDSEL0_IOLB</u>	32	GPIO GROUP IOLB TDSEL0 Control
00007F0C	<u>RDSEL0_IOLB</u>	32	GPIO GROUP IOLB RDSEL0 Control
00007F10	<u>PULLEN0_IOLB</u>	32	GPIO GROUP IOLB PULLEN0 Control
00007F14	<u>PULLSEL0_IOLB</u>	32	GPIO GROUP IOLB PULLSEL0 Control
00007F18	<u>DRV0_IOLB</u>	32	GPIO GROUP IOLB DRV0 Control

00007F00		<u>IES0_IOLB</u>										GPIO GROUP IOLB IES0 Control					0000007F
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	
Type																	
Reset																	
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Name											IES_IOLB_6_SMI_MDIO	IES_IOLB_5_SMI_MDC	IES_IOLB_4_LAN_0	IES_IOLB_3_LAN_1	IES_IOLB_2_LAN_2	IES_IOLB_1_LAN_3	IES_IOLB_0_LAN_4
Type											RW	RW	RW	RW	RW	RW	
Reset											1	1	1	1	1	1	

Bit(s)	Name	Description
6	IES_IOLB_6_SMI_MDIO	SMI_MDIO IES 0: Disable 1: Enable
5	IES_IOLB_5_SMI_MDC	SMI_MDC IES 0: Disable

Bit(s)	Name	Description
		1: Enable
4	IES_IOLB_4_LAN0_LED0	LAN0_LED0 IES 0: Disable 1: Enable
3	IES_IOLB_3_LAN0_LED1	LAN0_LED1 IES 0: Disable 1: Enable
2	IES_IOLB_2_LAN1_LED0	LAN1_LED0 IES 0: Disable 1: Enable
1	IES_IOLB_1_LAN1_LED1	LAN1_LED1 IES 0: Disable 1: Enable
0	IES_IOLB_0_LAN2_LED1	LAN2_LED1 IES 0: Disable 1: Enable

00007F04		SMT0_IOLB			GPIO GROUP IOLB SMT0 Control												00000020	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		

Name										SMT_IOLB_6_SMI_MDIO	SMT_IOLB_5_SMI_MDC	SMT_IOLB_4_LAN0_LED0	SMT_IOLB_3_LAN0_LED1	SMT_IOLB_2_LAN1_LED0	SMT_IOLB_1_LAN1_LED1	SMT_IOLB_0_LAN2_LED1
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	1	0	0	0	0	0

Bit(s)	Name	Description
6	SMT_IOLB_6_SMI_MDIO	SMI_MDIO SMT 0: Disable 1: Enable
5	SMT_IOLB_5_SMI_MDC	SMI_MDC SMT 0: Disable 1: Enable
4	SMT_IOLB_4_LAN0_LED0	LAN0_LED0 SMT 0: Disable 1: Enable
3	SMT_IOLB_3_LAN0_LED1	LAN0_LED1 SMT 0: Disable 1: Enable
2	SMT_IOLB_2_LAN1_LED0	LAN1_LED0 SMT 0: Disable 1: Enable
1	SMT_IOLB_1_LAN1_LED1	LAN1_LED1 SMT 0: Disable 1: Enable

Bit(s)	Name	Description
0	SMT_IOLB_0_LAN2_LED1	LAN2_LED1
		SMT
		0: Disable
		1: Enable

00007F08	TDSEL0_IOLB				GPIO GROUP IOLB TDSEL0 Control								0AAAAAAAA			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					TDSEL_IOLB_6_SMI_MDIO				TDSEL_IOLB_5_SMI_MDC				TDSEL_IOLB_4_LAN0_LED0			
Type					RW				RW				RW			
Reset					1	0	1	0	1	0	1	0	1	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	TDSEL_IOLB_3_LAN0_LED1				TDSEL_IOLB_2_LAN1_LED0				TDSEL_IOLB_1_LAN1_LED1				TDSEL_IOLB_0_LAN2_LED1			
Type	RW				RW				RW				RW			
Reset	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0

Bit(s)	Name	Description
27:24	TDSEL_IOLB_6_SMI_MDIO	SMI_MDIO
		TDSEL
23:20	TDSEL_IOLB_5_SMI_MDC	SMI_MDC
		TDSEL
19:16	TDSEL_IOLB_4_LAN0_LED0	LAN0_LED0
		TDSEL
15:12	TDSEL_IOLB_3_LAN0_LED1	LAN0_LED1
		TDSEL
11:8	TDSEL_IOLB_2_LAN1_LED0	LAN1_LED0
		TDSEL
7:4	TDSEL_IOLB_1_LAN1_LED1	LAN1_LED1
		TDSEL
3:0	TDSEL_IOLB_0_LAN2_LED1	LAN2_LED1

Bit(s)	Name	Description
		TDSEL

00007F0C RDSEL0 IOLB GPIO GROUP IOLB RDSEL0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name			RDSEL_IOLB_6_SMI_MDIO	RDSEL_IOLB_5_SMI_MDC	RDSEL_IOLB_4_LAN0_LED0	RDSEL_IOLB_3_LAN0_LED1	RDSEL_IOLB_2_LAN1_LED0	RDSEL_IOLB_1_LAN1_LED1	RDSEL_IOLB_0_LAN2_LED1							
Type			RW	RW	RW	RW	RW	RW	RW							
Reset			0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
13:12	RDSEL_IOLB_6_SMI_MDIO	SMI_MDIO RDSEL
11:10	RDSEL_IOLB_5_SMI_MDC	SMI_MDC RDSEL
9:8	RDSEL_IOLB_4_LAN0_LED0	LAN0_LED0 RDSEL
7:6	RDSEL_IOLB_3_LAN0_LED1	LAN0_LED1 RDSEL
5:4	RDSEL_IOLB_2_LAN1_LED0	LAN1_LED0 RDSEL
3:2	RDSEL_IOLB_1_LAN1_LED1	LAN1_LED1 RDSEL
1:0	RDSEL_IOLB_0_LAN2_LED1	LAN2_LED1 RDSEL

00007F10 PULLEN0_IOLB GPIO GROUP IOLB PULLEN0 Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PULLEN_IOLB_6_SMI_MDIO	PULLEN_IOLB_5_SMI_MDC	PULLEN_IOLB_4_LAN0_LED0	PULLEN_IOLB_3_LAN0_LED1	PULLEN_IOLB_2_LAN1_LED0	PULLEN_IOLB_1_LAN1_LED1	PULLEN_IOLB_0_LAN2_LED1
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	PULLEN_IOLB_6_SMI_MDIO	SMI_MDIO PULLEN 0:Disable pull control 1:Enable pull control
5	PULLEN_IOLB_5_SMI_MDC	SMI_MDC PULLEN 0:Disable pull control 1:Enable pull control
4	PULLEN_IOLB_4_LAN0_LED0	LAN0_LED0 PULLEN 0:Disable pull control 1:Enable pull control
3	PULLEN_IOLB_3_LAN0_LED1	LAN0_LED1 PULLEN 0:Disable pull control 1:Enable pull control
2	PULLEN_IOLB_2_LAN1_LED0	LAN1_LED0 PULLEN

Bit(s)	Name	Description
		0:Disable pull control
		1:Enable pull control
1	PULLEN_IOLB_1_LAN1_LED1	LAN1_LED1 PULLEN 0:Disable pull control 1:Enable pull control
0	PULLEN_IOLB_0_LAN2_LED1	LAN2_LED1 PULLEN 0:Disable pull control 1:Enable pull control

00007F14 PULLSELO_IOLB GPIO GROUP IOLB PULLSELO Control 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										PULLSE L_IOLB 6_SMI _MDIO	PULLSE L_IOLB 5_SMI _MDC	PULLSE L_IOLB 4_LAN 0_LED0	PULLSE L_IOLB 3_LAN 0_LED1	PULLSE L_IOLB 2_LAN 1_LED0	PULLSE L_IOLB 1_LAN 1_LED1	PULLSE L_IOLB _0_LA N2_LE D1
Type										RW	RW	RW	RW	RW	RW	RW
Reset										0	0	0	0	0	0	0

Bit(s)	Name	Description
6	PULLSEL_IOLB_6_SMI_MDIO	SMI_MDIO PULLSEL 0:Pull down select 1:Pull up select
5	PULLSEL_IOLB_5_SMI_MDC	SMI_MDC

Bit(s)	Name	Description
		PULLSEL
		0:Pull down select
		1:Pull up select
4	PULLSEL_IOLB_4_LAN0_LED0	LAN0_LED0
		PULLSEL
		0:Pull down select
		1:Pull up select
3	PULLSEL_IOLB_3_LAN0_LED1	LAN0_LED1
		PULLSEL
		0:Pull down select
		1:Pull up select
2	PULLSEL_IOLB_2_LAN1_LED0	LAN1_LED0
		PULLSEL
		0:Pull down select
		1:Pull up select
1	PULLSEL_IOLB_1_LAN1_LED1	LAN1_LED1
		PULLSEL
		0:Pull down select
		1:Pull up select
0	PULLSEL_IOLB_0_LAN2_LED1	LAN2_LED1
		PULLSEL
		0:Pull down select
		1:Pull up select

00007F18	GPIO GROUP IOLB DRV0 Control												02222222			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name					DRV_IOLB_6_SMI_MDIO				DRV_IOLB_5_SMI_MDC				DRV_IOLB_4_LAN0_LED0			
Type					RW				RW				RW			

Reset					0	0	1	0	0	0	1	0	0	0	1	0
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	DRV_IOLB_3_LAN0_LED1				DRV_IOLB_2_LAN1_LED0				DRV_IOLB_1_LAN1_LED1				DRV_IOLB_0_LAN2_LED1			
Type	RW				RW				RW				RW			
Reset	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit(s)	Name	Description
27:24	DRV_IOLB_6_SMI_MDIO	SMI_MDIO DRV
23:20	DRV_IOLB_5_SMI_MDC	SMI_MDC DRV
19:16	DRV_IOLB_4_LAN0_LED0	LAN0_LED0 DRV
15:12	DRV_IOLB_3_LAN0_LED1	LAN0_LED1 DRV
11:8	DRV_IOLB_2_LAN1_LED0	LAN1_LED0 DRV
7:4	DRV_IOLB_1_LAN1_LED1	LAN1_LED1 DRV
3:0	DRV_IOLB_0_LAN2_LED1	LAN2_LED1 DRV

11 GPHY

11.1 Register Definition

Module name: gephy_all Base address: (+0000000)

Address	Name	Width	Register Function
00000000	<u>Reg00h</u>	16	Mode Control Register
00000010	<u>Reg01h</u>	16	Mode Status Register
00000020	<u>Reg02h</u>	16	PHY Identifier 1 Register
00000030	<u>Reg03h</u>	16	PHY Identifier 2 Register
00000040	<u>Reg04h</u>	16	Auto-Negotiation Advertisement Register
00000050	<u>Reg05h</u>	16	Auto-Negotiation Link Partner Ability Register
00000060	<u>Reg06h</u>	16	Auto-Negotiation Expansion Register
00000070	<u>Reg07h</u>	16	Auto-Negotiation Next Page Transmit Register
00000080	<u>Reg08h</u>	16	Auto-Negotiation LP Next Page Receive Register
00000090	<u>Reg09h</u>	16	1000BASE-T Control Register
000000A0	<u>Reg0Ah</u>	16	1000BASE-T Status Register
000000D0	<u>Reg0dh</u>	16	MMD access control Register
000000E0	<u>Reg0eh</u>	16	MMD access address data Register
000000F0	<u>Reg0Fh</u>	16	1000BASE-T Status Extension 1 Register
51F00210	<u>dev1Fh_reg021h</u>	16	LED Basic Control Register
51F00220	<u>dev1Fh_reg022h</u>	16	LED On Duration Register
51F00230	<u>dev1Fh_reg023h</u>	16	LED Blinking Duration Register
51F00240	<u>dev1Fh_reg024h</u>	16	LED0 On Control Register
51F00250	<u>dev1Fh_reg025h</u>	16	LED0 Blinking Control Register
51F00260	<u>dev1Fh_reg026h</u>	16	LED1 On Control Register
51F00270	<u>dev1Fh_reg027h</u>	16	LED1 Blinking Control Register
507003C0	<u>dev07h_reg03Ch</u>	16	EEE Advertisement Register
507003D0	<u>dev07h_reg03Dh</u>	16	EEE LP Advertisement Register

00000000 Reg00h

Mode Control Register

00001040

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MainReset	Loopback	MrForceSpeedSelInt_0	MrAutonegEnableSMInt	Pwdn	IsolateInt	MrRestartAutoneg	MrDuplexModelInt	MrCollisionTestEn	MrForceSpeedSelInt_1						
Type	W1C	RW	RW	RW	RW	RW	W1C	RW	RW	RW						
Reset	0	0	0	1	0	0	0	0	0	1						

Bit(s)	Name	Description
15	MainReset	Software Reset 0:Reset de-asserted 1:Reset asserted
14	Loopback	Loopback 0:Loopback disabled 1:Loopback enabled
13	MrForceSpeedSelInt_0	Forced Speed Selection [LSB]MSB = bit6, LSB = bit1300: 10Mbps01: 100Mbps10: 1000Mbps11: Reserved
12	MrAutonegEnableSMInt	Auto-negotiation Enable 0:Auto-negotiation disabled. 1:Auto-negotiation enabled
11	Pwdn	Power-down 0:No effect 1:RGMII in-band signaling does not function
10	IsolateInt	Isolate 0:No effect 1:Disable MAC interface outputs and ignore MAC interface inputs
9	MrRestartAutoneg	Restart Auto-negotiation 0:No effect 1:Restart auto-negotiation
8	MrDuplexModelInt	Duplex

Bit(s)	Name	Description
		0:Half-duplex
		1:Full-duplex
7	MrCollisionTestEn	Collision Test Enable
		0:No effect
		1:Collision Test enabled
6	MrForceSpeedSelInt_1	Forced Speed Selection [MSB] See bit 13 above

00000010 **Reg01h** **Mode Status Register** 00007949

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	CAP_100T4	CAP_100X_FDX	CAP_100X_HDX	CAP_10T_FDX	CAP_10T_HDX	CAP_10T2_FDX	CAP_10T2_HDX	EXT_STA_EN		PRAM_SUP_CAP	MrAutonegCompleteRefClk	RemoteFaultRefClk	AN_CAP	LinkStatus	JabberActiveStateBit_sp_refclk	EXT_CAP
Type	RO	RO	RO	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO	RO
Reset	0	1	1	1	1	0	0	1		1	0	0	1	0	0	1

Bit(s)	Name	Description
15	CAP_100T4	100BASE-T4 Capability
		0:Not 100BASE-T4 capable
		1:100BASE-T4 capable
14	CAP_100X_FDX	100BASE-X FDX Capability
		0:Not 100BASE-X FDX capable
		1:100BASE-X FDX capable
13	CAP_100X_HDX	100BASE-X HDX Capability
		0:Not 100BASE-X HDX capable
		1:100BASE-X HDX capable
12	CAP_10T_FDX	10BASE-T FDX Capability
		0:Not 10BASE-T FDX capable

Bit(s)	Name	Description
		1:10BASE-T FDX capable
11	CAP_10T_HDX	10BASE-T HDX Capability 0:Not 10BASE-T HDX capable 1:10BASE-T HDX capable
10	CAP_100T2_FDX	100BASE-T2 FDX Capability 0:Not 100BASE-T2 FDX capable 1:100BASE-T2 FDX capable
9	CAP_100T2_HDX	100BASE-T2 HDX Capability 0:Not 100BASE-T2 HDX capable 1:100BASE-T2 HDX capable
8	EXT_STA_EN	Extended Status Enable 0:No effect 1:Extended status information present in register 15
6	PRAM_SUP_CAP	Preamble Suppression Capability 0:MF always required 1:MF preamble may be suppressed
5	MrAutonegComplete_RefClk	Auto-negotiation Complete 0:Auto-negotiation not complete 1:Auto-negotiation complete
4	RemoteFault_RefClk	Remote Fault 0:Far-end fault not detected 1:Far-end fault detected
3	AN_CAP	Auto-negotiation Capability 0:Auto-negotiation not capable 1:Auto-negotiation capable
2	LinkStatus	Link Status 0:Link is not up 1:Link is up
1	JabberActiveStateBit_sp_refclk	Jabber Detect 0:Jabber condition not detected 1:Jabber condition detected
0	EXT_CAP	Extended Capability

Bit(s)	Name	Description
		0:Extended register not capable
		1:Extended register capable

00000020 Reg02h PHY Identifier 1 Register 000003A2

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUI_I															
Type	RO															
Reset	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1	0

Bit(s)	Name	Description
15:0	OUI_I	Organizationally Unique Identifier [3:18]OUI bit 3 to bit 18

00000030 Reg03h PHY Identifier 2 Register 0000A412

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	OUI_u						PartNumber						RevCode			
Type	RO						RO						RO			
Reset	1	0	1	0	0	1	0	0	0	0	0	1	0	0	1	0

Bit(s)	Name	Description
15:10	OUI_u	Organizationally Unique Identifier [19:24]OUI bit 19 to bit 24
9:4	PartNumber	Part Number
3:0	RevCode	Revision Code

Bit(s)	Name	Description

00000040 Reg04h Auto-Negotiation Advertisement Register 00000DE1

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NextPageReq		SmiRf_CL28		Pause		AdvCap100T4	AdvCap100FDX	AdvCap100HDX	AdvCap10FDX	AdvCap10HDX	AdvSelector				
Type	RW		A0		RW		RW	RW	RW	RW	RW	RW				
Reset	0		0		1	1	0	1	1	1	1	0	0	0	0	1

Bit(s)	Name	Description

15 NextPageReq **Next Page Transmission Request**

0:Request disabled

1:Request enabled

13 SmiRf_CL28 **Transmit Remote Fault**

0:Disabled

1:Enabled

11:10 Pause **Advertise Asynchronous Pause**

9 AdvCap100T4 **Advertise 100BASE-T4**

0:No effect

1:Advertises 100BASE-T4

8 AdvCap100FDX **Advertise 100BASE-TX FDX**

0:No effect

1:Advertise 100BASE-TX FDX

7 AdvCap100HDX **Advertise 100BASE-TX HDX**

0:No effect

1:Advertise 100BASE-TX HDX

6 AdvCap10FDX **Advertise 10BASE-T FDX**

0:No effect

Bit(s)	Name	Description
		1:Advertise 10BASE-T FDX
5	AdvCap10HDX	Advertise 10BASE-T HDX 0:No effect 1:Advertise 10BASE-T HDX
4:0	AdvSelector	Advertise Selector 5'h00: Reserved for future Auto-negotiation development 5'h01: IEEE Std 802.3 5'h02: IEEE Std 802.9 ISLAN-16T 5'h1F: Reserved for future Auto-negotiation development

00000050			Reg05h		Auto-Negotiation Link Partner Ability Register												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	LpNextPageTxReq_RefClk	Lp_Ack_RefClk	LpCapRF_final_RefClk	LpReservedTech_RefClk	LpCapPause_RefClk		LpCap100T4_RefClk	LpCap100FDX_RefClk	LpCap100HDX_RefClk	LpCap100FDX_RefClk	LpCap100HDX_RefClk	LpSelector_RefClk							
Type	RO	RO	RO	RO	RO		RO	RO	RO	RO	RO	RO							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15	LpNextPageTxReq_RefClk	LP Next Page Transmission Request 0:Not Requested 1:Requested
14	Lp_Ack_RefClk	LP Acknowledge 0:No effect 1:Acknowledge
13	LpCapRF_final_RefClk	LP Remote Fault 0:No effect 1:Remote fault

Bit(s)	Name	Description
12	LpReservedTech_RefClk	LP Reserved Technologies Reserved for future technology
11:10	LpCapPause_RefClk	LP Advertise Asynchronous Pause
9	LpCap100T4_RefClk	LP Advertise 100BASE-T4 0:No effect 1:Capable of 100BASE-T4
8	LpCap100FDX_RefClk	LP Advertise 100BASE-TX FDX 0:No effect 1:Capable of 100BASE-TX FDX
7	LpCap100HDX_RefClk	LP Advertise 100BASE-TX HDX 0:No effect 1:Capable of 100BASE-TX HDX
6	LpCap10FDX_RefClk	LP Advertise 10BASE-T FDX 0:No effect 1:Capable of 10BASE-T FDX
5	LpCap10HDX_RefClk	LP Advertise 10BASE-T HDX 0:No effect 1:Capable of 10BASE-T HDX
4:0	LpSelector_RefClk	LP Advertise Selector 5'h00: Reserved for future Auto-negotiation development 5'h01: IEEE Std 802.3 5'h02: IEEE Std 802.9 ISLAN-16T 5'h1F: Reserved for future Auto-negotiation development

00000060		Reg06h				Auto-Negotiation Expansion Register											00000004	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name												MrParallelDetectFault	MrLnPAbLe_RefClk	MrNpAbLe	MrNewPageRxSMI	MrLnPAbLe_RefClk		

												t_RefCl k				
Type												RO	RO	RO	RC	RO
Reset												0	0	1	0	0

Bit(s)	Name	Description
4	MrParallelDetectFault_RefClk	Parallel Detection Fault 0:No effect 1:Parallel detection fault
3	MrLpNpAble_RefClk	LP Next Page Capable 0:No effect 1:LP is next page capable
2	MrNpAble	Local PHY Next Page Capable 0:No effect 1:Local PHY is next page capable
1	MrNewPageRxSMI	Page Received 0:No effect 1:New page has been received
0	MrLpAutonegAble_RefClk	LP Auto-negotiation Capable 0:No effect 1:LP is capable of auto-negotiation

00000070 Reg07h Auto-Negotiation Next Page Transmit Register 00002001

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	NP		MSG_P G	ACK2	MrTog gleTx_ RefClk	MSG_UF_CODE										
Type	RW		RW	RW	RO	RW										
Reset	0		1	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit(s)	Name	Description
15	NP	Next Page 0:No effect 1:More pages follow
13	MSG_PG	Message Page 0:Unformatted page 1:Message page
12	ACK2	Acknowledge 2 0:Cannot comply with request. 1:Complies with request
11	MrToggleTx_RefClk	Toggle 0:Previous transmitted LCW = 1 (LCW: Link Code Word) 1:Previous transmitted LCW = 0
10:0	MSG_UF_CODE	Message/unformatted Code Content of message/unformatted page

00000080			Reg08h		Auto-Negotiation LP Next Page Receive Register												00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name	LP_NP	LP_ACK	LP_MSG	LP_ACK2	LP_MrToggle	LP_MSG_UF_CODE												
Type	RO	RO	RO	RO	RO	RO												
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
15	LP_NP	LP Next Page 0:No effect 1:More pages follow
14	LP_ACK	Acknowledge 0:No effect

Bit(s)	Name	Description
		1:LP acknowledge
13	LP_MSG	LP Message Page 0:Unformatted page 1:Message page
12	LP_ACK2	LP Acknowledge 2 0:LP cannot comply with request 1:LP complies with request
11	LP_MrToggle	LP Toggle 0:Previous transmitted LCW = 1 (LCW: Link Code Word) 1:Previous transmitted LCW = 0
10:0	LP_MSG_UF_CODE	LP Message /unformatted Code Content of message/unformatted page

00000090				Reg09h				1000BASE-T Control Register								00000200			
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	tx_test_mode			MSCon fEnInt	MSCon fValInt	port_ty pe	AdvCap 1000FD X	AdvCap 1000H DX											
Type	RW			RW	RW	RW	RW	RW											
Reset	0	0	0	0	0	0	1	0											

Bit(s)	Name	Description
15:13	tx_test_mode	Transmitter test mode 000:Normal 001:Mode 1: Transmit waveform test 010:Mode 2: Transmit jitter test as master 011:Mode 3: Transmit jitter test as slave 100:Mode 4: Transmitter distortion test 101-111:Reserved: Operation not defined

Bit(s)	Name	Description
12	MSConfEnInt	Master/Slave manual configuration 0:No effect 1:Master/Slave manual configuration enabled
11	MSConfValInt	Master/Slave value (This register is only valid when bit 9.12 is set to 1) 0:Configure PHY as slave during negotiation 1:Configure PHY as master during negotiation
10	port_type	Port type 0:Single port device 1:Multi port device
9	AdvCap1000FDX	1000BASE-T FDX capability 0:No effect 1:PHY is 1000BASE-T FDX capable
8	AdvCap1000HDX	1000BASE-T HDX capability 0:No effect 1:PHY is 1000BASE-T HDX capable

000000A0		Reg0Ah		1000BASE-T Status Register												00004000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	MrMSConfigFault_RefClk	MSConf1000_RefClk	LocRcvrStatus1000_RefClk	RemRcvrStatus1000_RefClk	LpCap1000FDX_RefClk	LpCap1000HDX_RefClk			IdleErrCount1000_RefClk							
Type	RO	RO	RO	RO	RO	RO			RO							
Reset	0	1	0	0	0	0			0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15	MrMSConfigFault_RefClk	Master/Slave configuration fault (This bit latches high) 0:No master/slave configuration fault detected

Bit(s)	Name	Description
		1:Master/Slave configuration fault detected
14	MSConfig1000_RefClk	Master/Slave configuration resolution 0:Local PHY configuration resolved to slave 1:Local PHY configuration resolved to master
13	LocRcvrStatus1000_RefClk	Local receiver status 0:Local receiver not OK 1:Local receiver OK
12	RemRcvrStatus1000_RefClk	Remote receiver status 0:Remote receiver not OK 1:Remote receiver OK
11	LpCap1000FDX_RefClk	LP 1000BASE-T FDX capability 0:LP 1000BASE-T No FDX capable 1:LP 1000BASE-T FDX capable
10	LpCap1000HDX_RefClk	LP 1000BASE-T HDX capability 0:LP 1000BASE-T No HDX capable 1:LP 1000BASE-T HDX capable
7:0	IdleErrCount1000_RefClk	Idle error count

000000D0			Reg0dh		MMD access control Register												00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	mmd_op_mode											devAddr_c22							
Type	RW											RW							
Reset	0	0										0	0	0	0	0			

Bit(s)	Name	Description
15:14	mmd_op_mode	13.1513.14

Bit(s)	Name	Description
		00= address
		01= data, no post increment
		10= data, post increment on reads and writes
		11= data, post increment on writes only
4:0	devAddr_c22	Device address

000000E0			Reg0eh			MMD access address data Register											00000000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			
Name	mmd_addr_data																		
Type	OTHER																		
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0			

Bit(s)	Name	Description
15:0	mmd_addr_data	If 13.15:14 = 00, MMD DEVAD address register. Otherwise, MMD DEVAD data register is indicated by the contents of its address register 00= address 01= data, no post increment 10= data, post increment on reads and writes 11= data, post increment on writes only

000000F0		Reg0Fh			1000BASE-T Status Extension 1 Register												00003000		
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16			
Name																			
Type																			
Reset																			
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0			

Name	GIGA_X_FDX_CAP	GIGA_X_HDX_CAP	GIGA_T_FDX_CAP	GIGA_T_HDX_CAP												
Type	RO	RO	RO	RO												
Reset	0	0	1	1												

Bit(s)	Name	Description
15	GIGA_X_FDX_CAP	1000BASE-X FDX capability 0:No 1000BASE-X FDX capability 1:PHY is 1000BASE-X FDX capability
14	GIGA_X_HDX_CAP	1000BASE-X HDX capability 0:No 1000BASE-X HDX capability 1:PHY is 1000BASE-X HDX capability
13	GIGA_T_FDX_CAP	1000BASE-T FDX capability 0:No 1000BASE-X FDX capability 1:PHY is 1000BASE-T FDX capability
12	GIGA_T_HDX_CAP	1000BASE-T HDX capability 0:No 1000BASE-X HDX capability 1:PHY is 1000BASE-T HDX capability

51F00210 dev1Fh reg021h				LED Basic Control Register												0000000B
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	led_enhance_mode											led_event_all	Led_Clock_Enable	Led_Timing_Test	led_mode	
Type	RW											RW	RW	RW	RW	
Reset	0											0	1	0	1	1

Bit(s)	Name	Description
15	led_enhance_mode	Extended Control

Bit(s)	Name	Description
		0:LED functions are controlled by 2-bit LED_MODE field of this register
		1:LED functions of each pin are independently controlled by LED0_ON_CTL~LED3_ON_CTL and LED0_BLK_CTL~LED3_BLK_CTL
4	led_event_all	Use all port LED event
3	Led_Clock_Enab	LED Clock Enable
		LED Timing Test
		0:Disable LED clock
		1:Enable LED clock
2	Led_Timing_Test	LED Timing Test
		0:Normal LED clock frequency
		1:Increase LED clock frequency
1:0	led_mode	LED Mode Configuration.
		00b:All LED outputs are disabled.
		01b:2 LED pins are enabled, active high LED0: Link. LED1: Activity. Each LED pin polarity is automatically configured. Note: the above settings can also be achieved by setting the following register fields when EXT_CTL=1 LED0_ON_CTL' Status = 7'b0000111 LED0_BLK_CTL' Event = 10'b0000000000 LED1_ON_CTL' Status = 7'b00000000 LED1_BLK_CTL' Event = 10'b0000111111
		10b:3 LED pins are enabled, active high. LED0: Link1000 Activity. LED1: Link100 Activity. LED2: Link10 Activity Each LED pin polarity is automatically configured.Note: the above settings can also be achieved by setting following register fields when EXT_CTL=1LED0_ON_CTL' Status = 7'b0000001LED0_BLK_CTL' Event = 10'b0000000011LED1_ON_CTL' Status = 7'b0000010LED1_BLK_CTL' Event = 10'b0000001100LED2_ON_CTL' Status = 7'b0000100LED2_BLK_CTL' Event = 10'b0000110000
		11b:3 LED pins are enabled, active high. LED0: Link1000 Activity. LED1: Link10/100 Activity. LED2: Duplex/Collision Each LED pin polarity is automatically configured.Note: the above settings can also be achieved by setting following register fields when EXT_CTL=1LED0_ON_CTL' Status = 7'b0000001LED0_BLK_CTL' Event = 10'b0000000011LED1_ON_CTL' Status = 7'b0000110LED1_BLK_CTL' Event = 10'b0000111100LED2_ON_CTL' Status = 7'b0010000LED2_BLK_CTL' Event = 10'b0001000000

51F00220	dev1Fh_reg022h				LED On Duration Register												00000C00
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	
Name																	

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	led_on_dur															
Type	RW															
Reset	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	led_on_dur	LED on Duration LED ON duration in terms of number of 32.768 us. 32.768 us~2.147 sec period. Default value = 0x0C00 * 32.768 us = 100.66 ms

51F00230 dev1Fh_reg023h LED Blinking Duration Register 00001400

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	led_blk_dur															
Type	RW															
Reset	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
15:0	led_blk_dur	LED Blinking Duration Blinking Periodic duration in terms of number of 32.768 us. 32.768 us ~ 2.147 sec period Default value = 0x1400 * 32.768 us = 167.77 ms

51F00240 dev1Fh_reg024h LED0 On Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																

Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led0_en	rg_led0_pol								led0_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led0_en	Enable Ethernet LED Function. 0: Disable (Hi-Z) 1: Enable
14	rg_led0_pol	Select LED polarity. This field only takes effect when LED_EN is 1b1. Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led0_on_mask	LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1. Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00250	dev1Fh	reg025h	LED0 Blinking Control Register													00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Name						led0_blk_mask									
Type						RW									
Reset						0	0	0	0	0	0	0	0	0	0

Bit(s)	Name	Description
9:0	led0_blk_mask	LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1. (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter what LED-On status is) Bit[0]:1000Mbps TX Activity Bit[1]:1000Mbps RX Activity Bit[2]:100Mbps TX Activity Bit[3]:100Mbps RX Activity Bit[4]:10Mbps TX Activity Bit[5]:10Mbps RX Activity Bit[6]:Collision Bit[7]:RX CRC Error Bit[8]:RX Idle Error Bit[9]:Force Blinks (Logic 1)

51F00260 dev1Fh_reg026h LED1 On Control Register 00008000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name	rg_led1_en	rg_led1_pol								led1_on_mask						
Type	RW	RW								RW						
Reset	1	0								0	0	0	0	0	0	0

Bit(s)	Name	Description
15	rg_led1_en	Enable Ethernet LED Function.

Bit(s)	Name	Description
		0: Disable (Hi-Z)
		1: Enable
14	rg_led1_pol	Select LED polarity. This field only takes effect when LED_EN is 1b1. Enable Ethernet LED Function. 0: Active low (That is, LED On means Output 0) 1: Active high (That is, LED On means Output 1)
6:0	led1_on_mask	LED is on if any of the following state holds. This field only takes effect when LED_EN is 1b1. Select LED polarity. This field only takes effect when LED_EN is 1b1. Bit[0]:Link 1000 Bit[1]:Link 100 Bit[2]:Link 10 Bit[3]:Link Down Bit[4]:Full Duplex Bit[5]:Half Duplex Bit[6]:Force On (Logic 1)

51F00270		dev1Fh_reg027h				LED1 Blinking Control Register											00000000	
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16		
Name																		
Type																		
Reset																		
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Name							led1_blk_mask											
Type							RW											
Reset							0	0	0	0	0	0	0	0	0	0		

Bit(s)	Name	Description
9:0	led1_blk_mask	LED blinks if any of the following event occurs. This field only takes effect when LED_EN is 1b1. (Notes: The LED-Blinking Priority Precedes The LED-On Priority, That is, when there is an event that triggers LED-Blinking, it will take control of LED output no matter LED-On status is)

Bit(s)	Name	Description
		Bit[0]:1000Mbps TX Activity
		Bit[1]:1000Mbps RX Activity
		Bit[2]:100Mbps TX Activity
		Bit[3]:100Mbps RX Activity
		Bit[4]:10Mbps TX Activity
		Bit[5]:10Mbps RX Activity
		Bit[6]:Collision
		Bit[7]:RX CRC Error
		Bit[8]:RX Idle Error
		Bit[9]:Force Blinks (Logic 1)

507003C0 dev07h_reg03Ch EEE Advertisement Register 00000000

Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										adv_ee_e_10g_kr	adv_ee_e_10g_kx4	adv_ee_e_1g_kx	adv_ee_e_10g_t	adv_ee_e_1g_t_pre	adv_ee_e_100m_tx_pre	
Type										RW	RW	RW	RW	RW	RW	
Reset										0	0	0	0	0	0	

Bit(s)	Name	Description
6	adv_eee_10g_kr	10GBase-KR EEE 0: Do not advertise that the 10GBASE-KR has EEE capability 1: Advertise that the 10GBASE-KR has EEE capability
5	adv_eee_10g_kx4	10GBase-KX4 EEE 0: Do not advertise that the 10GBASE-KX4 has EEE capability 1: Advertise that the 10GBASE-KX4 has EEE capability
4	adv_eee_1g_kx	1000Base-KX EEE 0: Do not advertise that the 1000BASE-KX has EEE capability

Bit(s)	Name	Description
3	adv_eee_10g_t	1: Advertise that the 1000BASE-KX has EEE capability 10GBase-T EEE 0: Do not advertise that the 10GBASE-T has EEE capability 1: Advertise that the 10GBASE-T has EEE capability
2	adv_eee_1g_t_pre	1000Base-T EEE 0: Do not advertise that the 1000BASE-T has EEE capability 1: Advertise that the 1000BASE-T has EEE capability
1	adv_eee_100m_tx_pre	100Base-TX EEE 0: Do not advertise that the 100BASE-TX has EEE capability 1: Advertise that the 100BASE-TX has EEE capability

507003D0		dev07h_reg03Dh				EEE LP Advertisement Register										00000000
Bit	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Name																
Type																
Reset																
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Name										lp_eee_10g_kr	lp_eee_10g_kx4	lp_eee_1g_kx	lp_eee_10g_t	lp_eee_1g_t	lp_eee_100m_tx	
Type										RO	RO	RO	RO	RO	RO	
Reset										0	0	0	0	0	0	

Bit(s)	Name	Description
6	lp_eee_10g_kr	10GBase-KR EEE 0: Link partner is not advertising EEE capability for 10GBASE-KR 1: Link partner is advertising EEE capability for 10GBASE-KR
5	lp_eee_10g_kx4	10GBase-KX4 EEE 0: Link partner is not advertising EEE capability for 10GBASE-KX4 1: Link partner is advertising EEE capability for 10GBASE-KX4
4	lp_eee_1g_kx	1000Base-KX EEE 0: Link partner is not advertising EEE capability for 1000BASE-KX

Bit(s)	Name	Description
3	lp_eee_10g_t	1: Link partner is advertising EEE capability for 1000BASE-KX 10GBase-T EEE 0: Link partner is not advertising EEE capability for 10GBASE-T
2	lp_eee_1g_t	1: Link partner is advertising EEE capability for 10GBASE-T 1000Base-T EEE 0: Link partner is not advertising EEE capability for 1000BASE-T
1	lp_eee_100m_tx	1: Link partner is advertising EEE capability for 100BASE-T 100Base-TX EEE 0: Link partner is not advertising EEE capability for 100BASE-TX 1: Link partner is advertising EEE capability for 100BASE-TX

11.2 Programming Guide

11.2.1 Self-Control LED

Normally, user can use the default LED_MODE ([dev1Fh_reg021h](#)[1:0]) to indicate GPHY status. Below is the supported four kinds of LED flash behavior.

00b: All LED outputs are disabled

01b:2 LED pins are enabled, active high.LED0: Link. LED1: Activity.

10b:3 LED pins are enabled, active high. LED0: Link1000 Activity. LED1: Link100 Activity. (LED2 not supported)

11b:3 LED pins are enabled, active high. LED0: Link1000 Activity. LED1: Link10/100 Activity. (LED2 not supported)

For some customers, they could require more LED flash behavior than LED_MODE can support. GPHY provides the following programming guide to enable the self-control LED and show the required flash behavior.

1. Configure LED_ENHANCE_MODE=1 on GPHY REG [dev1Fh_reg021h](#)[15] to enable the self-control LED.
2. For LED0, the corresponding programming CR is [dev1Fh_reg024h](#) and [dev1Fh_reg025h](#)
3. For LED1, the corresponding programming CR is [dev1Fh_reg026h](#) and [dev1Fh_reg027h](#)
4. To enable LED0 and set the suggested polarity, please set [dev1Fh_reg024h](#)[15]=1 and [dev1Fh_reg024h](#)[14]=1
5. LED0 On mask bits ([dev1Fh_reg024h](#)[6:0]) provide the status bits to turn on LED.
6. LED0 Blinking mask bits ([dev1Fh_reg025h](#)[9:0]) provide the status bits to be blinking.
7. On MT7531 reference board, LED pins usually has the strap function through the external pull-up/down resistor. The final LED signal drives the active high/low based on the pull resistor.

0x7808[12]	Dev1Fh_reg024h (LED0)	LED0 pin strap	LED0 drive	Dev1Fh_reg026h (LED1)	LED1 pin strap	LED1 drive
0 (LED1 follows LED0)	[15]: LED enable [14]: Active-High	Pull-Up	Active-Low	[15]: LED enable [14]: Active-High	--	Active-Low
		Pull-Down	Active-High		--	Active-High
1 (LED1 drives by LED1 strap)	[15]: LED enable [14]: Active-High	Pull-Up	Active-Low	[15]: LED enable [14]: Active-High	Pull-Up	Active-Low
		Pull-Down	Active-High		Pull-Down	Active-High

Table 11-1 Relative LED control on LED final drive signal.